1995-06

Single event upsets and noise margin enhancement of gallium arsenide Pseudo-Complimentary MESFET Logic

Van Dyk, Steven E.

Monterey, California. Naval Postgraduate School

NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

THESIS

SINGLE EVENT UPSETS AND NOISE MARGIN ENHANCEMENT OF GALLIUM ARSENIDE PSEUDO-COMPLIMENTARY MESFET LOGIC

By

Steven E. Van Dyk

June, 1995

Thesis Advisor: Douglas J. Fouts

Approved for public release; distribution is unlimited.

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 June 1995	Master's Thesis

4. SINGLE EVENT UPSETS AND NOISE MARGIN ENHANCEMENT OF GALLIUM ARSENIDE PSEUDO-COMPLIMENTARY MESFET LOGIC.	5. FUNDING NUMBERS
6. AUTHOR(S) Steven E. Van Dyk	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey CA 93943-5000	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT	12b. DISTRIBUTION CODE
Approved for public release; distribution is unlimited.	

13. ABSTRACT *(maximum 200 words)*

The use of gallium arsenide (GaAs) logic circuits in high performance computers and digital systems in space applications is desirable due to their high speed and immunity to total dose radiation. Several problem areas must be overcome for more widespread use. First, GaAs MESFETs with short gate lengths are susceptible to single event upsets (SEU) in a high radiation environment and second, GaAs circuits consume relatively large amounts of static power. To overcome the shortcomings of these areas, a new type of GaAs logic family called Pseudo-Complementary MESFET Logic (PCML) was designed. This new type of GaAs logic consumes less power than current logic families and provides improved tolerances to SEUs. Experiments which estimated the charge required to generate SEUs in PCML circuits are described. The power consumption of a test circuit using PCML is analyzed and the data presented for a caparison against other GaAs logic families. Further refinements to PCML are discussed.

14. SUBJECT TERMS Single Event Upset, Gallium Arsenide Logic			15. NUMBER OF PAGES * 70 16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18 298-102

Approved for public release; distribution is unlimited.

SINGLE EVENT UPSETS AND NOISE MARGIN ENHANCEMENT OF GALLIUM ARSENIDE PSEUDO-COMPLIMENTARY MESFET LOGIC

Steven E. Van Dyk
Lieutenant Commander, United States Navy
B.S., University of Southern California, 1980

Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
June 1995

Author: [redacted]
Steven E. Van Dyk

Approved by: [redacted]
Douglas J. Fouts, Thesis Advisor

[redacted]
Herschel Loomis, Second Reader

[redacted]
Michael A. Morgan, Chairman
Department of Electrical Engineering

ABSTRACT

The use of gallium arsenide (GaAs) logic circuits in high performance computers and digital systems in space applications is desirable due to their high speed and immunity to total dose radiation. Several problem areas must be overcome for more widespread use. First, GaAs MESFETs with short gate lengths are susceptible to single event upsets (SEU) in a high radiation environment and second, GaAs circuits consume relatively large amounts of static power. To overcome the shortcomings of these areas, a new type of GaAs logic family called Pseudo-Complementary MESFET Logic (PCML) was designed. This new type of GaAs logic consumes less power than current logic families and provides improved tolerances to SEUs. Experiments which estimate the charge required to generate SEUs in PCML circuits are described. The power consumption of a test circuit using PCML is analyzed and the data presented for a caparison against other GaAs logic families. Further refinements to PCML are discussed.

TABLE OF CONTENTS

I. INTRODUCTION 1

A. GALLIUM ARSENIDE 1

B. GALLIUM ARSENIDE DIGITAL LOGIC 3

1. Direct-Coupled FET Logic 3

2. Two-Phase Dynamic FET Logic 5

3. Pseudo-Complimentary MESFET Logic 6

II. SINGLE EVENT UPSET TESTING 9

A. BACKGROUND 9

B. TESTING FIXTURE DESIGN 10

C. TESTING PROCEDURES AND EQUIPMENT 19

D. TEST RESULTS AND ANALYSIS 25

III. PCML GALLIUM ARSENIDE CIRCUIT TESTING 31

A. BACKGROUND 31

B. TESTING FIXTURE MODIFICATION 33

C. TESTING PROCEDURES AND EQUIPMENT 33

D. TEST RESULTS AND ANALYSIS 35

IV. PROPOSED IMPROVEMENTS TO PCML 45

A. PROBLEM AREAS 45

B. PROPOSED SOLUTIONS AND INITIAL RESULTS 45

V. COMMENTS AND CONCLUSIONS 57

A. SINGLE EVENT UPSET TESTING 57

B. PSEUDO-COMPLIMENTARY MESFET LOGIC CIRCUIT TESTING 57

C. RECOMMENDATIONS FOR FUTURE RESEARCH 58

LIST OF REFERENCES 59

INITIAL DISTRIBUTION LIST 61

I. INTRODUCTION

A. GALLIUM ARSENIDE

During the last three decades, the microelectronic industry has been dominated by devices made of silicon. Advances in silicon device and circuit technology are continually being made. This dominance as the most used semiconductor is sure to continue. Recently however, another semiconductor material has been finding use in digital applications that require extremely high speeds of operation and/or resistance to high total-dose levels of ionizing radiation. Gallium arsenide (GaAs) is a compound formed by using gallium (third column of the periodic table of elements) and arsenic (fifth column of the periodic table of elements), therefore GaAs is referred to as a III-V semiconductor. [Ref 1]

Electrons travel much faster in *n*-type GaAs material than in silicon. This is due to the fact that the electron drift mobility μ_n is five to ten times higher in GaAs than in silicon. Thus, for the same bias conditions, GaAs devices will have a higher output current which will result in a higher g_m compared to a silicon device. The larger output current allows for faster charging and discharging of load and parasitic capacitance which results in increased speed of operation. [Ref 1] The Cray Computer Corporation CRAY-3 Supercomputer used GaAs integrated circuits for all its logic circuits and attained a clock speed of 480 MHz [Ref 2].

GaAs circuits can tolerate higher total-dose levels (approximately 10^8 rads) of ionizing radiation than silicon (approximately 10^6 rads) [Ref 3]. This immunity to the effects of slowly accumulating radiation allows a GaAs device to have little or no shielding. This attribute makes GaAs circuits particularly attractive for space craft and military applications [Ref 4]. Unfortunately, GaAs MESFETs with short gate lengths (on the order of one micron) have demonstrated susceptibility to single event upsets (SEUs) in high radiation environments. SEUs are transient in nature and caused because of an increased charge collection at the edges of the gate called "edge effects" [Ref 5]. The

source of the charge can be α-particles, protons, or heavy ions striking the GaAs substrate. If the collision is in the vicinity of a transistor and a charge of sufficient magnitude is deposited, it can cause the logic gate output to change logic values. This can cause a cascading error effect on subsequent bistable circuitry. [Ref 3] As the trend toward smaller device sizes operating at higher switching speeds continues, the probability of a SEU occurrence also increases.

The basic GaAs circuit technology uses a *n*-channel field effect transistor (FET) known as a metal semiconductor FET or MESFET and a Schottky-barrier diode (SBD). Unlike silicon complimentary metal oxide semiconductor (CMOS) devices the GaAs *p*-channel FETs are so slow compared to *n*-channel FETs that they are not used as pull-up transistors. The structure of a MESFET and SBD are illustrated by their cross sections, shown in Figure 1. A GaAs circuit is built on an undoped GaAs substrate. Conductivity of undoped GaAs is very low and the substrate is considered semi-insulating. This characteristic simplifies the process of isolating devices from each other on the same chip and results in a smaller parasitic capacitance between devices and circuit ground. [Ref 1]

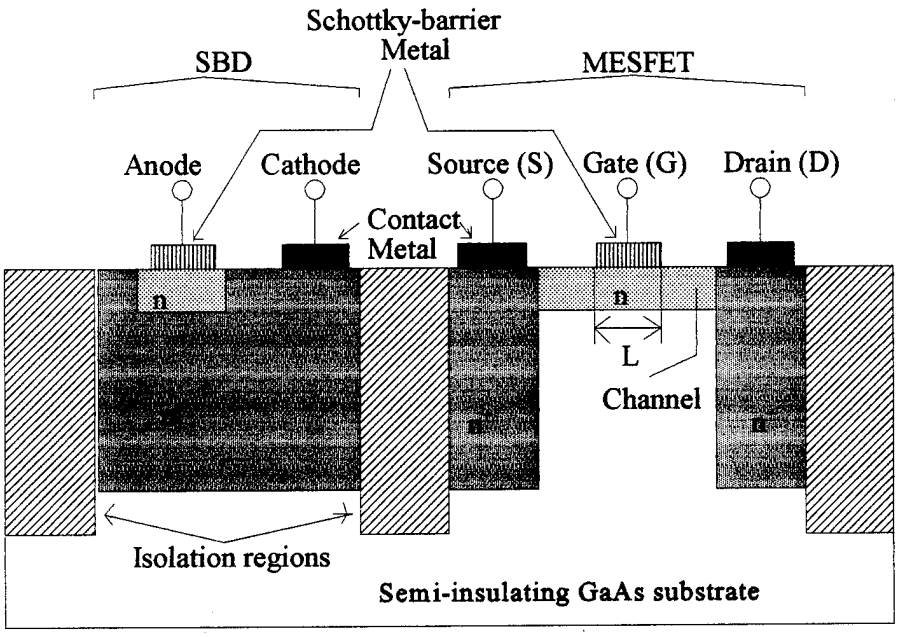


Figure 1 Cross Section of a GaAs SBD and a MESFET.

The Schottky-barrier diode consists of a Schottky-barrier metal which forms the anode and *n*-type GaAs which forms the cathode. It should be mentioned, the Schottky-barrier metal is different from the metal used to make the other contacts. A heavily doped *n*-type GaAs (indicated by n^+) is used between the *n* region and the cathode metal contact in order to keep the parasitic series resistance low. [Ref 1]

The MESFET gate is formed by a Schottky-barrier metal in direct contact with the *n*-type GaAs that forms the channel region. The channel length L is defined by the length of the gate electrode. Channel width W (in the direction perpendicular to the page) is defined the same way. To reduce the parasitic resistances between the drain and source contacts and the channel, the two contacts are surrounded with heavily doped (n^+) GaAs. The MESFET becomes operational when a depletion region is formed in the channel below the gate. This depletion region is formed and its thickness controlled by the gate voltage v_{GS}. Current flows from the drain to the source in response to an applied voltage between the drain and source v_{DS}. Eventually this voltage will cause the MESFET to enter the pinch-off region at the drain end of the channel. [Ref 1]

B. GALLIUM ARSENIDE DIGITAL LOGIC

GaAs logic offers the shortest propagation delays and, at equivalent operating speeds, a lower power consumption than all other types of logic families. Two currently used GaAs logic families, direct-coupled FET logic and two-phase dynamic FET logic, and a new GaAs logic family, called pseudo-complimentary MESFET logic, will be discussed.

1. Direct-Coupled FET Logic

Direct-coupled FET logic (DCFL) is the simplest form of GaAs digital logic circuits. Due to not being able to have *p*-channel and *n*-channel devices, large amounts of static power are consumed by static GaAs DCFL circuits. DCFL circuits

have shown a high susceptibility to SEUs [Ref 6]. A DCFL circuit utilizes enhancement MESFETs for the input switching transistors and a depletion MESFET for the load transistor. To understand how a DCFL circuit operates, consider the basic inverter schematic shown in Figure 2.

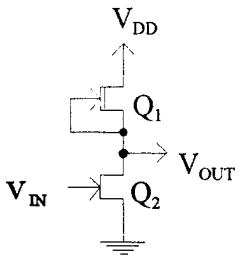


Figure 2 DCFL Inverter Schematic.

When V_{IN} is lower than the threshold voltage of the enhancement MESFET Q_2, the transistor is off. If the inverter's output was driving another device, current would flow from V_{DD} through the depletion MESFET Q_1 and into the gate of the next device. Since the gate to source junction of a GaAs MESFET is a Schottky-barrier diode, it will have a voltage drop of about 0.7 V when conducting. The high output voltage will therefore be clamped to about 0.7 V. As V_{IN} is increased above its threshold voltage the enhancement MESFET Q_2 turns on and starts to draw current. The output voltage will remain constant until the current through Q_2 equals the output current and then decrease to about 0.0 V. The output voltage swing of a DCFL MESFET circuit will be less than 0.7 V and current will always be flowing from V_{DD} to ground either through Q_2 or the load device. [Ref 1]

The constant current flow of DCFL MESFET circuits causes an excessive power consumption, typically 0.5 mW/gate. This limits the number of devices which can be placed on a single chip. For example, if an integrated circuit is constructed with DCFL gates which dissipate 0.5 mW each and they are placed in a package that can

dissipate 10 W, then it could contain no more than 20,000 gates. Lower power dissipation can be realized but at the expense of speed. [Ref 7]

2. Two-Phase Dynamic FET Logic

Two-phase dynamic FET logic (TDFL) is a ratio-less dynamic logic family that uses two nonoverlapping clocks and two power supplies. One power supply is used to power the gates (1.0 V or greater) and another is required for clock generators and drivers on those circuits that have on-chip clock generation (toggles between -1.2 and 0 V). One of the advantages of TDFL is that power is only dissipated during clock-level transitions. [Ref 7] TDFL circuits have shown a slightly lower susceptibility to SEUs than DCFL circuits [Ref 8].

To understand how a TDFL circuit operates, consider the basic inverter schematic shown in Figure 3.

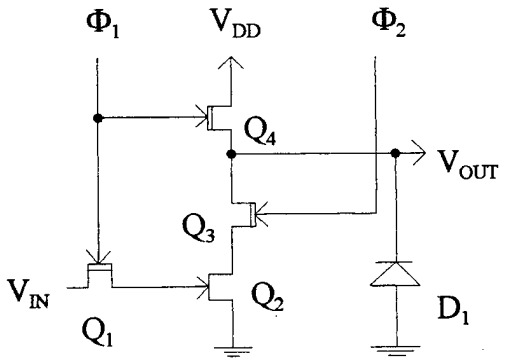


Figure 3 TDFL Inverter Schematic.

When Φ_1 is high, transistors Q_1 and Q_4 conduct causing V_{OUT} to charge to about 1.0 V. The output of Q_1 is charged to 0.6 V if the input is high or discharged to 0.0 V if the input is low. After Φ_1 goes low, Φ_2 goes high and Q_3 conducts. If the input was high during Φ_1, then Q_2 conducts and the output is discharged to ground. Had the input

been low during Φ_1, then Q_2 remains off and the output remains high. Since this output would be connected to another TDFL device, the voltage swing would actually be from 0.0 to 0.6 V due to the gate to source conduction of the next device. The output of a gate is not available until one-half clock cycle after the input has arrived. This delay has the disadvantage of allowing logic signals to propagate through one level of gates only every half clock cycle. Shift registers are used in pipelined architectures and compensate for this problem. TDFL gates are compatible with DCFL gates and can be connected together. [Ref 7]

Because TDFL is fully dynamic, current flows only during clock transitions. This means that power dissipation is proportional to the frequency. A TDFL inverter operating at 500 MHz, using a V_{DD} of 1.0 V and a clock swing voltage of 1.2 V has an average power consumption of 22 μW [Ref 7]. Using the same example used for DCFL, if an integrated circuit is constructed with TDFL gates which dissipate 22 μW each and they are placed in a package that can dissipate 10 W, then it could contain approximately 454,000 gates.

3. Pseudo-Complimentary MESFET Logic

Pseudo-complimentary MESFET logic (PCML) is a new GaAs logic family which is constructed using an all enhanced FET design and complimentary input and output nodes. The logic family consists of all the standard logic functions (not, nand, nor). Lieutenant Wolf's [Ref 9] simulation of PCML circuits indicated that they would have a much lower susceptibility to SEUs than either DCFL or TDFL circuits and this will be further investigated and reported on in Chapter II.

The basic idea behind the design of the PCML family is that one of the output nodes is always pulled to V_{DD} while the other output node is always pulled to ground. This is accomplished by having the outputs controlled by transistors which are either on and operating in the saturation region with low channel resistance, or off. The output does not depend upon clocks to shift a stored charge form one node to another as

in TDFL. Nor is there the large static current associated with DCFL. Operation of PCML gates is similar to that of silicon CMOS devices in that there is no static current flow between V_{DD} and ground. Power only flows when the logic gate is changing states, not every clock cycle as in TDFL. Lieutenant Wolf [Ref 9] believed that the total power consumption should be greatly reduced from that experienced by DCFL and TDFL circuits, this will be discussed in Chapter III.

To understand the basic operation of a PCML circuit, consider the inverter shown in Figure 4.

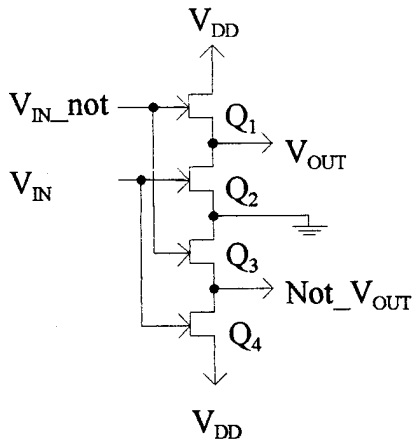


Figure 4 PCML Inverter Schematic.

When V_{IN} is high, V_{IN}_not will be low and Q_2 and Q_4 will be on and Q_1 and Q_3 will be off. This will cause the complimentary outputs, V_{OUT} to be pulled toward ground and not_V_{OUT} to be pulled toward V_{DD}. If V_{IN} is low, V_{IN}_not will be high and Q_1 and Q_3 will be on and Q_2 and Q_4 will be off. The complimentary outputs, V_{OUT} will be pulled toward V_{DD} and not_V_{OUT} will be pulled toward ground. Since these outputs would be connected to another PCML device, the voltage swing would actually be from 0.0 to 0.6 V due to the gate to source conduction of the next device. PCML gates are compatible with DCFL and TDFL gates and all three types can be interconnected.

One problem area with a PCML inverter reported by LT. Wolf [Ref 9] was the low DC gained it achieved, which results in poor noise margins. The DC transfer characteristic of a PCML inverter with a four inverter load on its output is illustrated in Figure 5. Chapter IV will include proposed improvements to the PCML family. HSPICE [Ref 10] will be used to verify if an improvement in the DC noise margin is possible.

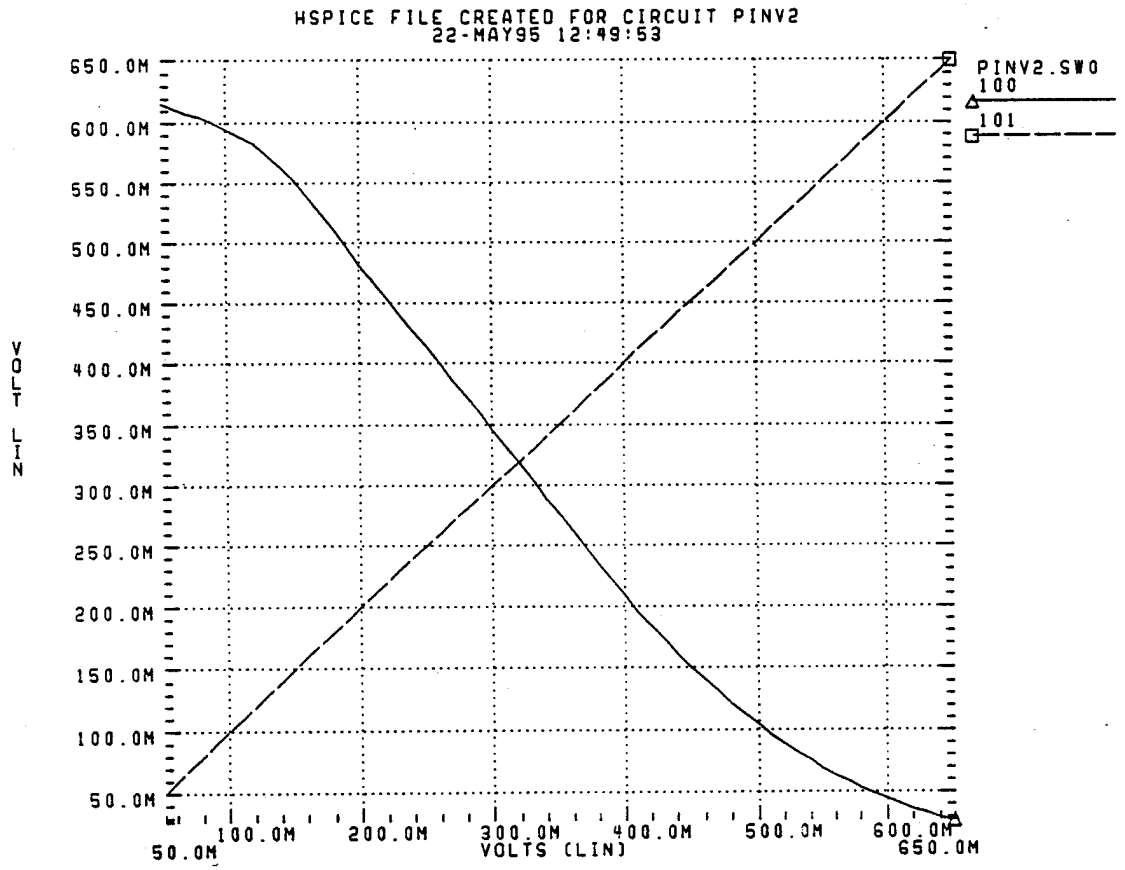


Figure 5 DC Transfer Characteristic of a PCML Inverter From Ref. [9].

Chapter V presents conclusions and recommendations for further use and testing of PCML circuits.

II. SINGLE EVENT UPSET TESTING

A. BACKGROUND

A charge build up on the critical node of a GaAs circuit, due to the effect of ionizing radiation, is the cause of single event upsets. LT K. Wolf and Professor D. J. Fouts [Ref 9] speculated that, if the majority of the energy imparted to a circuit, by a potential SEU, could be absorbed by the power source driving the logic gate, it would be reasonable to assume that the event would have a much smaller effect on the design performance of the circuit. It was from this thought and others that the PCML family was developed.

PCML is a new circuit topology which uses dual-path logic and is compatible with existing GaAs fabrication processes. The dual-path logic design allows one output to be pulled toward V_{DD} and the other toward ground. This provides a path to sink a large amount of current through the on transistors. Therefore, the resulting voltage transient on the output node of the circuit should be minimized. Since only one output node would be affected and complimentary outputs are always available, a critical operation could be monitored by an exclusive-OR of the outputs.

To further characterize and test the operation of PCML circuits, LT Wolf [Ref 9] designed a test and evaluation integrated chip using HSPICE and MAGIC [Ref 11]. In addition to PCML circuits, the chip contains DCFL and TDFL circuits and several test structures which the Navy Research Lab will use for other testing. The integrated circuit design was then fabricated at Vitesse Semiconductor Corporation using their standard, HGaAs-III, E/D MESFET fabrication process. The nominal transistor threshold voltage using this process is approximately +0.25 V for the enhancement-mode FETs used in the PCML circuits. The completed chip's layout is shown in Figure 6.

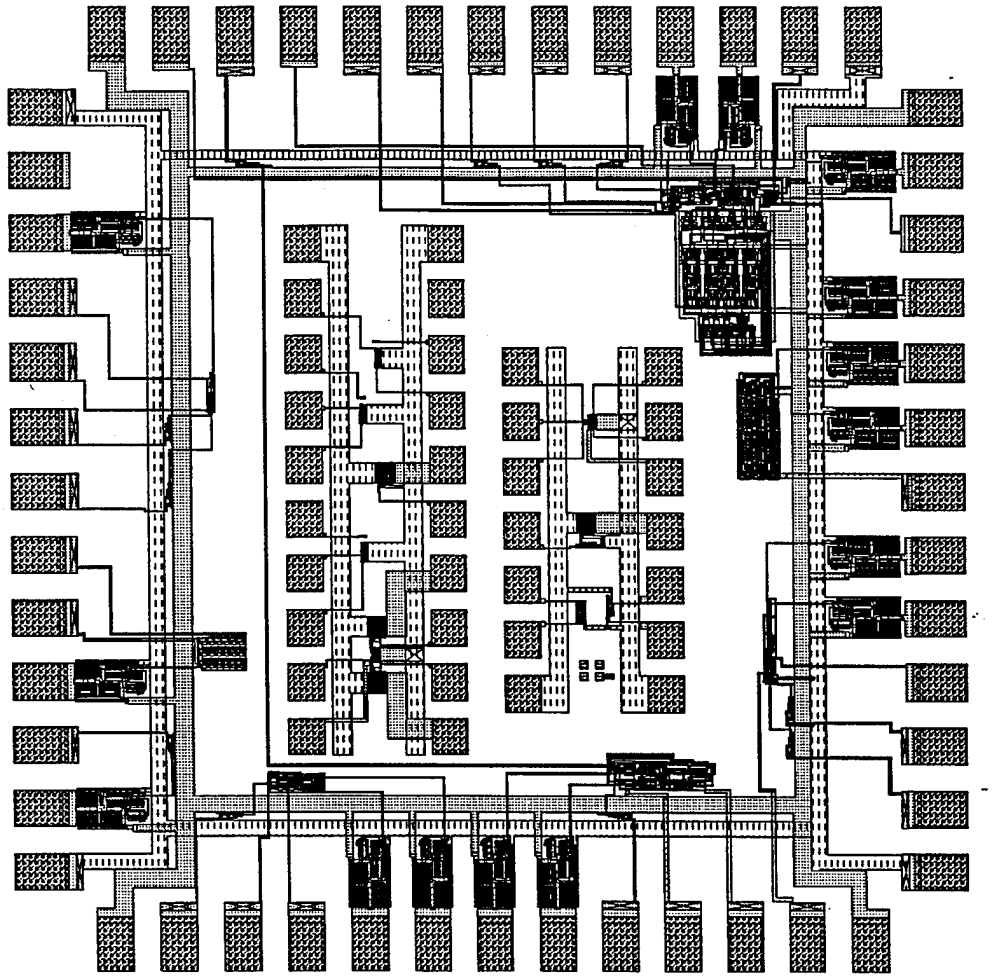


Figure 6 Completed Chip Layout From Ref. [9].

B. TESTING FIXTURE DESIGN

In order to conduct the SEU testing, a test fixture needed to be built which would hold the package containing the chip. One of the constraints in designing the test fixture was that it would have to fit in the SEU test set up at the Naval Research Lab in Washington, D.C. A size of four by six inches was chosen as a compromise between

minimizing size and ensuring stability. Stability was important because any movement of the target site during testing was unacceptable.

Figure 7 is the bonding diagram which was used to assist in the design of the test figure. From the bonding diagram and the chip's layout, the inputs and outputs of the pins were identified (Table 1A -C). To allow the test fixture to be used for testing of the DCFL and TDFL circuits, if desired, the board was constructed so their inputs and outputs were available.

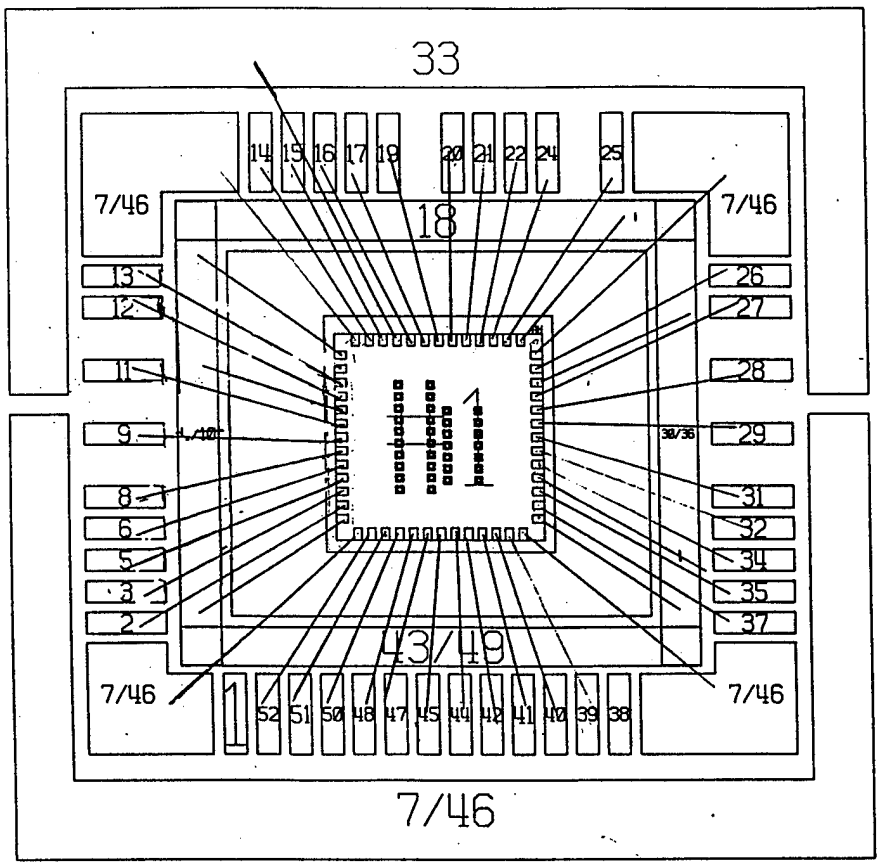


Figure 7 Bonding Diagram From Ref. [9].

Pin #	Pin Name	Meaning
1	PAD V_{DD}	Package GND
2	RECDRIV (Out)	Receiver driver output for testing the receiver driver to verify proper operation
3	RECDRIV (In)	Receiver driver input for testing the receiver driver to verify proper operation
4	PAD V_{DD}	Package GND
5	DCFL Ring (Out)	DCFL ring oscillator output
6	DCFL Ring GND	DCFL ring oscillator ground
7	PAD GND	Package V- (supply 1)
8	DCFL Ring V_{DD}	DCFL ring oscillator V_{DD}
9	DCFL SEU A (In)	DCFL test circuit input "A"
10	DCFL SEU V_{DD}	DCFL test circuit V_{DD} (PAD V_{DD})
11	DCFL SEU B (In)	DCFL test circuit input "B"
12	DCFL SEU GND	DCFL test circuit ground
13	DCFL SEU (Out)	DCFL test circuit output
14	FFLOP2 INIT (In)	Initializes FDML flip-flop
15	PFFLOP CLK NOT	PCML flip-flop not clock input
16	FSEU V_{DD}	FDML test circuit V_{DD}
17	FSEU GND	FDML test circuit ground
18	PAD V_{DD}	Package GND
19	Clock (In)	FDML 4-phase clock input
20	FSEU B (In)	FDML test circuit input "B"
21	FSEU A (In)	FDML test circuit input "A"

Table 1A Complete Pin Out of Test Chip.

Pin #	Pin Name	Meaning
22	FSEU A Not (Out)	FDML test circuit output "not A"
23	Substrate	Substrate voltage input
24	FSEU A (Out)	FDML test circuit output "A"
25	FFLOP2 GND	FDML flip-flop ground
26	FFLOP2 A Not (Out)	FDML flip-flop output "not A"
27	FFLOP2 A (Out)	FDML flip-flop output "A"
28	PRING A (Out)	PCML ring oscillator output "A"
29	PRING A Not (Out)	PCML ring oscillator output "not A"
30	FFLOP2 V_{DD}	FDML flip-flop V_{DD} (Package GND)
31	PRING V_{DD}	PCML ring oscillator V_{DD}
32	PRING A Not (Out)	PCML ring oscillator output "not A"
33	CLOCK Vss	Package Voltage Supply 2 (FDML 4-phase clock Vss input)
34	PSEU A (Out)	PCML test circuit output "A"
35	PSEU A (In)	PCML test circuit input "A"
36	PAD V_{DD}	Package GND
37	PSEU B (In)	PCML test circuit input "B"
38	Not Used	
39	PSEU GND	PCML test circuit ground
40	PFFLOP V_{DD}	PCML flip-flop V_{DD}
41	PFFLOP GND	PCML flip-flop ground
42	PFFLOP CLK	PCML flip-flop clock input
43	PAD V_{DD}	Package GND

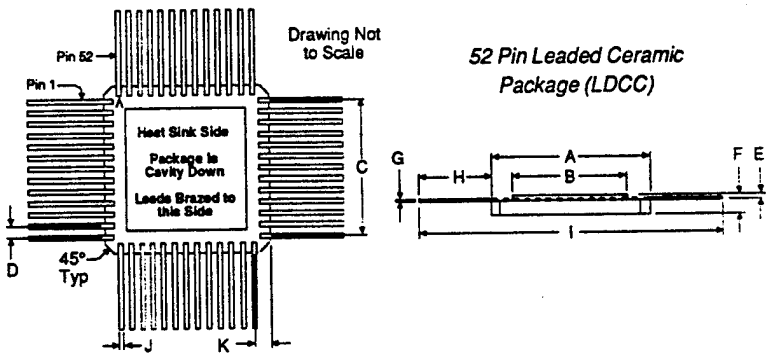
Table 1B Complete Pin Out of Test Chip.

Pin #	Pin Name	Meaning
44	PFFLOP Test 1	PCML flip-flop test node 1
45	PFFLOP Test 3	PCML flip-flop test node 3
46	PAD GND	Package V- (supply 1)
47	DFFLOP Q (Out)	DCFL flip-flop output "Q"
48	DFFLOP Q Not (Out)	DCFL flip-flop output "Q not"
49	PAD V_{DD}	Package GND
50	DFFLOP GND	DCFL flip-flop ground
51	DFFLOP V_{DD}	DCFL flip-flop V_{DD}
52	DFFLOP CLK	DCFL flip-flop clock input

Table 1C Complete Pin Out of Test Chip.

The integrated circuit was packaged in a 52-pin leaded ceramic flat pack (shown in Figure 8).

52 Pin Leaded Package (for FURY VSC3K only)



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	18.54/19.56	0.730/0.770	G	0.09/0.24	0.003/0.009
B	12.700/13.208	0.500/0.520	H	5.84/6.10	0.230/0.240
C*	15.24 TYP	0.600 TYP	I	31.75 TYP	1.25 TYP
D*	1.27 TYP	0.050 TYP	J	0.36/0.56	0.014/0.022
E	0.41/0.61	0.016/0.024	K*	1.75/1.90	0.069/0.075
F	2.03/2.79	0.080/0.110			

* At package body.

Figure 8 52 Pin Leaded Ceramic Package From Ref. [12]

Coaxial cable connects the test equipment and inputs to the test fixture. All inputs are terminated into 50Ω chip type microwave resistors. This reduces reflections and cross talk and allows for operation at high frequencies. To allow for easier soldering of the coaxial cable, pads with a width of 50 mils and a center to center distance of 100 mils were needed. This meant the 20 mils wide leads, which had a center to center distance of 50 mils, would have to be fanned out to meet the output pads. Since the chip would be operating at high frequencies, the distance from the package leads to the pads was minimized and the angle of the bends was kept as small as possible. A preliminary sketch was drawn, starting with 13 output pads which were than fanned in using 45^0 angles until they connected to 13 package leads.

Although the chip was designed to function with V_{DD} equal to +3.3 V and ground equal to 0.0 V, the decision was made to have chip V_{DD} equal to +1.65 V and chip ground equal to -1.65 V with a termination ring at true ground. This allows the monitoring of the outputs on oscilloscopes with 50Ω terminated inputs. This minimizes reflections and cross talk at the high frequencies the chip is tested at. In an effort to maintain the four by six inch size, individual power, ground and termination rings were constructed on the bottom of the board. A termination ring was also placed on the top of the board for the coaxial connections. The pins on the top of the board, which would need to be attached to the power and ground rings on the bottom, were connected using vias. This arrangement required the pad length to be 150 mils to allow the via connections to properly lineup. Additionally, the termination ring on the top was connected to the termination ring on the bottom through four via connections.

Since the chip would be operating at high frequencies, it was believed the chip would generate significant heat. To allow the heat sink to function properly and dissipate the heat, it was necessary to have the heat sink up and the lid placed against the test fixture. The problem with this approach was, how could the lid be removed and the laser light be directed at individual transistors? The solution decided on was to cut a hole (.75 inches square) in the test fixture. This approach would allow for maximum

heat dissipation, maximum contact between the package leads and the test fixture, and easy removal of the lid for testing.

The actual test fixture layout was accomplished using TangoPCB Plus Version 2.1 [Ref. 13] using the preliminary sketch and ring layout as a guide. The Tango layout of the top and bottom of the board are shown in Figures 9 and 10, respectively. After the Tango layout was completed, a Gerber file and aperture list was created to allow the board to be milled. Milling of the board was accomplished at the Naval Postgraduate School using the Space System Academic Group's LPKF Type 101 P Circuit Board Milling Machine using a 12 mil cutting tool and 31.5 mil drill.

V_{DD} and ground power supply connections were made using coaxial cable, with the center connected to the appropriate ring and the shield connected to the termination ring on the bottom of the fixture. Chip type microwave capacitors were used for bypassing high frequency noise on the power, ground and termination rings. The coaxial cable used for the inputs and outputs were soldered with the center connected to the pad and the shield connected to the termination ring. The appropriate via connections were made and the test fixture completed. The top and bottom views of the completed board are shown in Figures 11 and 12, respectively.

To secure the chip to the test fixture and allow for the testing of several chips, an aluminum clamp, padded with felt and secured with four screws, was manufactured.

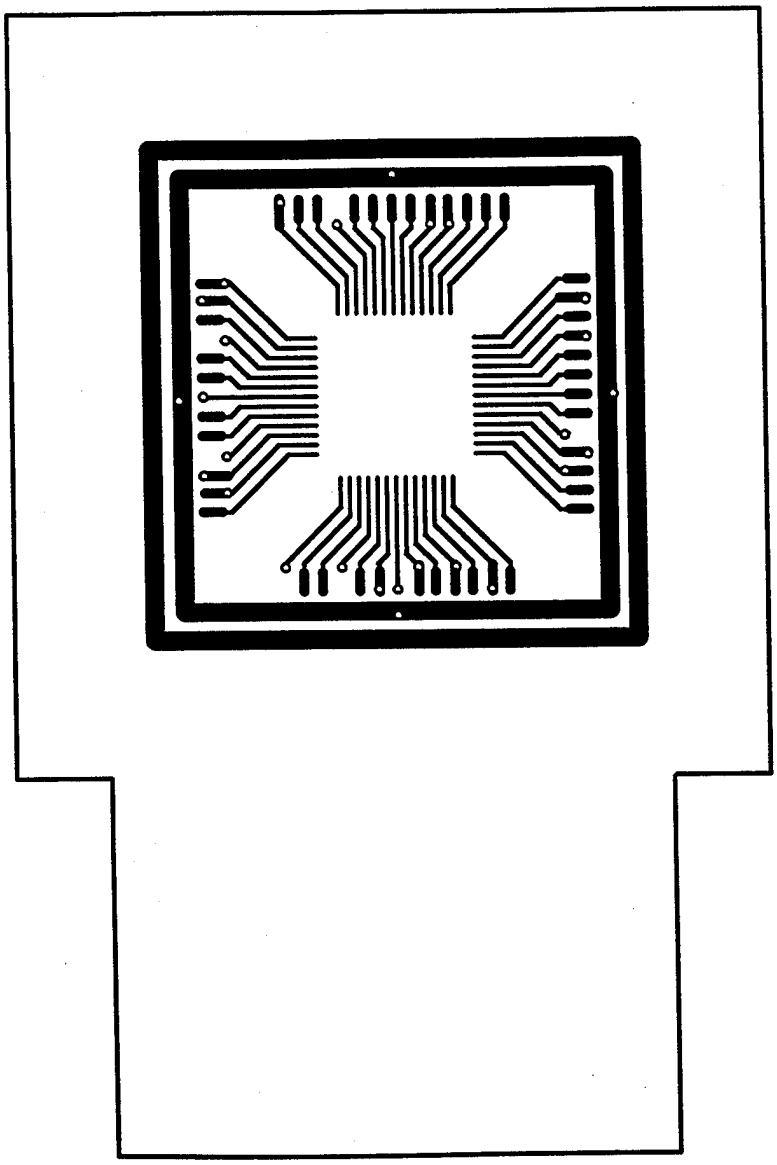


Figure 9 Tango Layout of the Top of Test Fixture.

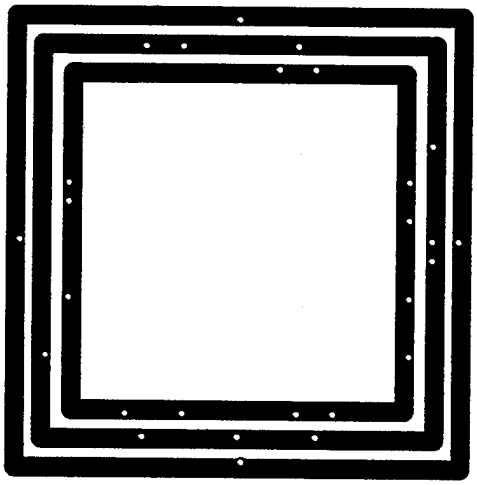


Figure 10 Tango Layout of the Bottom of Test Fixture.

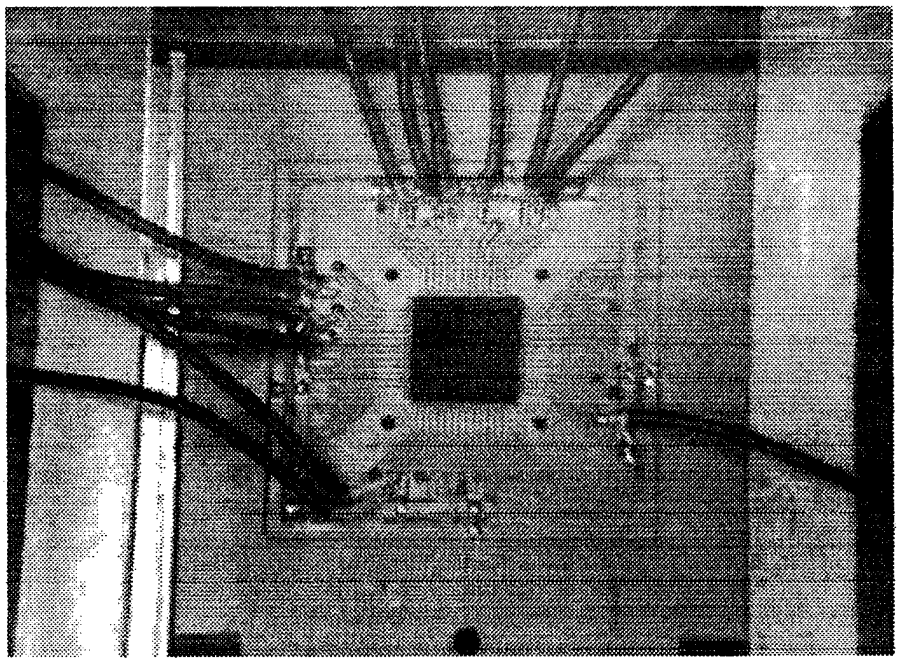


Figure 11 Top View of Test Fixture.

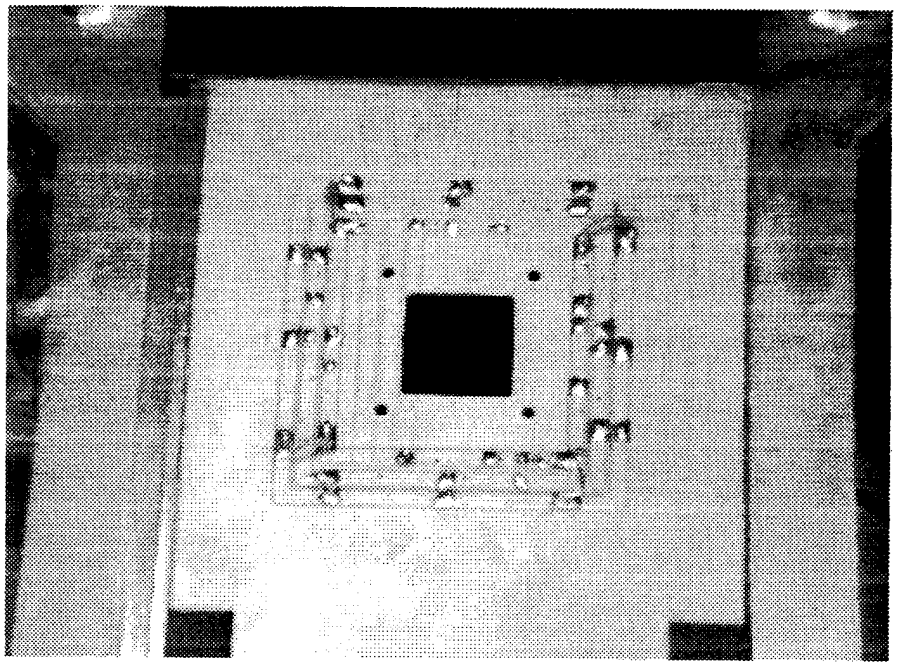


Figure 12 Bottom View of Test Fixture.

C. TESTING PROCEDURES AND EQUIPMENT

If any transistor in a PCML logic gate experiences a charge collection event (SEU), then the output logic value of that gate could be effected. Electrons are attracted toward regions of positive potential such as the drain of a transistor, and holes are attracted toward regions of negative potential such as the source of a transistor [Ref 14]. Therefore, in the laser experiments described here, it was necessary to determine the sensitivity of each transistor in a gate in order to determine the soft error rate for the entire gate. The gates chosen were two inverters and a NOR gate in the SEU test circuit (Figure 13) and an inverter in the 35 stage ring oscillator (Figure 14). The mask layout of the inverter is shown in Figure 15 and the NOR gate is shown in Figure 16 [Ref 14]. A

legend for the stipple patterns used in Figures 15 and 16 is shown in Figure 17. Laser target locations are annotated in both Figures 15 and 16, and verbal descriptions of the target locations are provided in Tables 2 and 3.

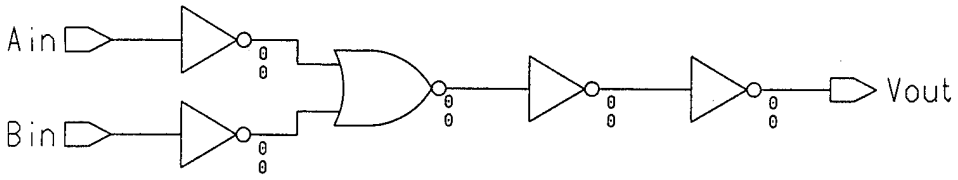


Figure 13 SEU Test Structure Schematic From Ref. [9]

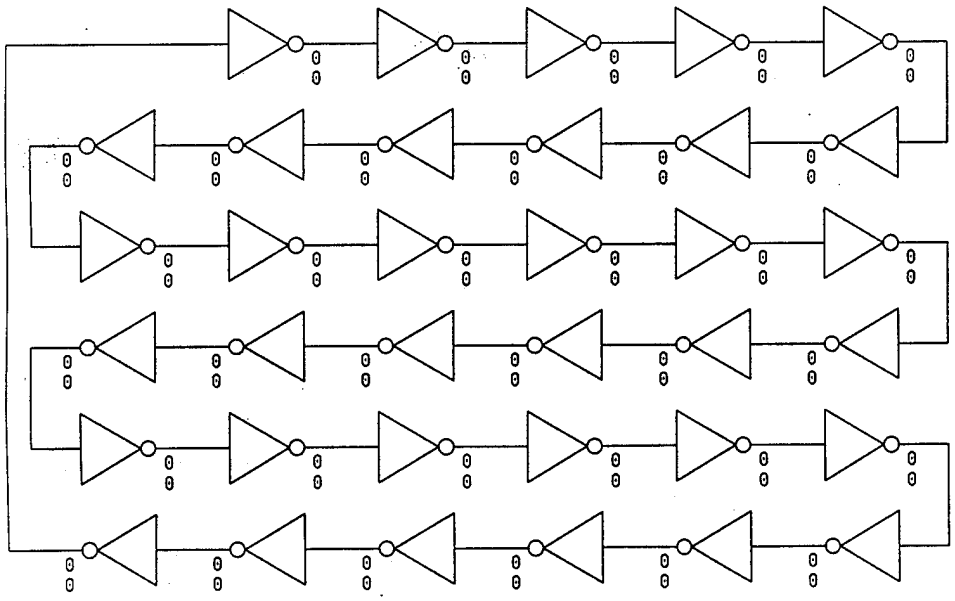


Figure 14 Ring Oscillator Schematic From Ref. [9].

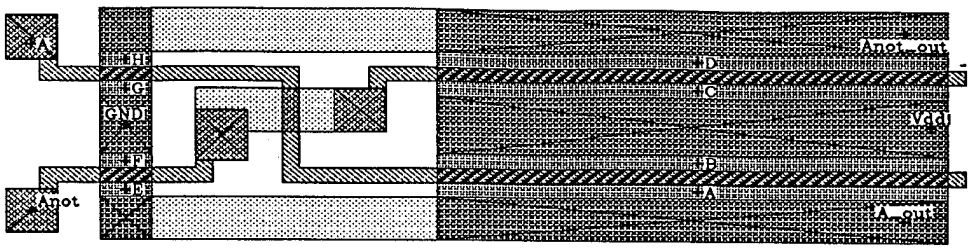


Figure 15 Inverter Layout From Ref. [14].

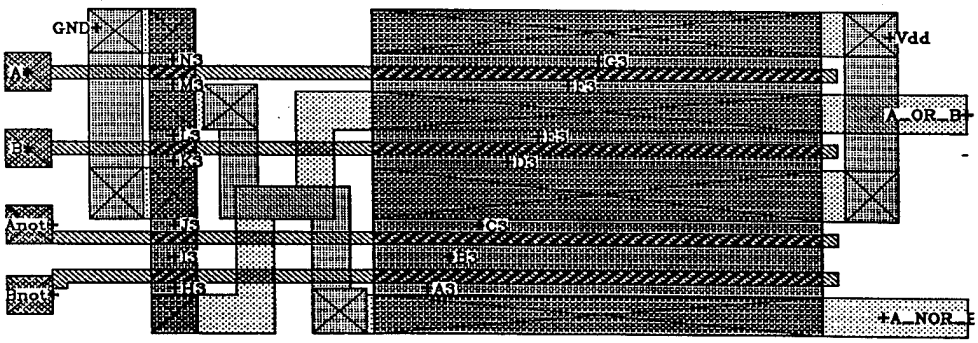


Figure 16 NOR Gate Layout From Ref.[14].

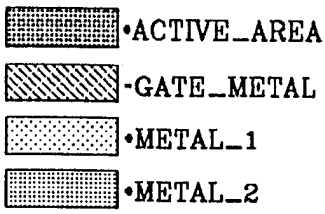


Figure 17 Stipple Pattern.

Laser Target	Target Location
A	in channel on source side of gate of Q_1
B	in channel on drain side of gate of Q_1
C	in channel on drain side of gate of Q_4
D	in channel on source side of gate of Q_4
E	in channel on drain side of gate of Q_2
F	in channel on source side of gate of Q_2
G	in channel on source side of gate of Q_3
H	in channel on drain side of gate of Q_3

Table 2 Laser Target Locations for Inverters From Ref. [14].

Laser Target	Target Location
A3	in channel on source side of gate of Q_1
B3	in channel between dual gates of Q_1
C3	in channel on drain side of gate of Q_1
D3	in channel on drain side of gate of Q_6
E3	in channel on source side of gate of Q_6
F3	in channel on source side of gate of Q_5
G3	in channel on drain side of gate of Q_5
H3	in channel on drain side of gate of Q_4
I3	in channel between dual gates of Q_4
J3	in channel on source side of gate of Q_4
K3	in channel on source side of gate of Q_3
L3	in channel on drain side of gate of Q_3
M3	in channel on drain side of gate of Q_2
N3	in channel on source side of gate of Q_2

Table 3 Laser Target Locations for NOR Gate From Ref [14].

Figure 18 shows the bottom of the test fixture with the integrated circuit installed and the lip open. Figure 19 shows the top of the test fixture with the integrated circuit chip installed. The lid was left unsealed so it could be removed and allow laser light to illuminate the chip. Charge-collection events were induced with the output of a modelocked, cavity-dumped, dye laser centered at 620 nm (2.0 eV). The use of a pulse laser in charge collection experiments, for testing the SEU characteristics of devices and circuits, is well documented [Refs 15, 16, 17, 18], as are the limitations of the method [Ref 19, 20, 21]. The pulse repetition rate of the laser used in the experiments described

here was 12.198 kHz, with a pulse duration of 1 ps. Spot size was approximately 1 μm in diameter.

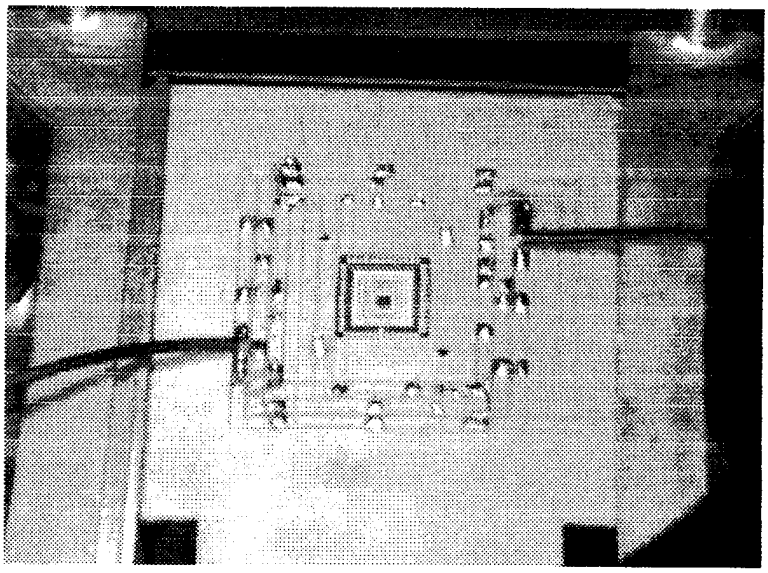


Figure 18 Bottom of Test Fixture.

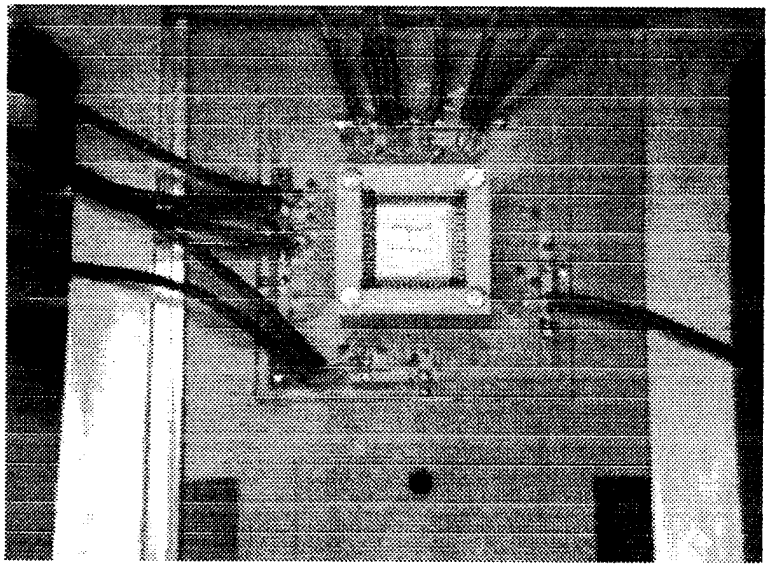


Figure 19 Top of Test Figure.

From the laser energies measured during the experiment, the amount of charge created in the semiconductor from the laser pulse can be calculated. Irradiating with 620 nm light corresponds to an absorption coefficient $\alpha = 5 \times 10^4/cm$, and the 1/e absorption depth is approximately 0.2μm below the surface. It is assumed that each photon absorbed by the GaAs creates a single electron-hole pair, and any remnant photon energy is converted to phonons (heat). It is also assumed that approximately 67% of the incident light is absorbed in the GaAs. The rest is reflected at the air/overglass and overglass/GaAs boundaries.

The output of the test circuit was measured using a Tektronix 11801A digitizing sampling oscilloscope with a bandwidth of 18GHz. Using power supply voltages of +1.65 V for V_{DD} and -1.65 V for ground, the on-chip logic levels were approximately -1.6V for a logic 0 and -1.1V for a logic 1. Off-chip logic levels were -1.0V for a logic 0 and +0.4V for a logic 1.

D. TEST RESULTS AND ANALYSIS

Prior to conducting any experiments using the laser to induce an SEU, each test circuit was tested to ensure it functioned properly. The first circuit tested was an inverter in the SEU test circuit with the A and B inputs held at a constant logic 1 value. The oscilloscope was monitored to detect a transition on the outputs. Results of the test are presented in Table 4.

The second circuit tested was a second inverter in the SEU test circuit with the A and B inputs held at a constant logic 0 value. The oscilloscope was monitored to detect a transition on the outputs. Results of the test are presented in Table 5.

Laser Target Location	Deposited Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A	0.53	51.2	2.91×10^{-7}
B	0.07	51.2	1.85×10^{-5}
C	10.18	51.2	8.00×10^{-10}
D	7.34	51.2	1.54×10^{-9}
E	166.9	8.0	4.66×10^{-13}
F	0.18	8.0	3.83×10^{-7}
G	36.72	8.0	9.62×10^{-12}
H	11.52	8.0	9.78×10^{-11}

Table 4 SEU Sensitivities of Inverter Circuit with Logic 1 Input From Ref. [14].

Laser Target Location	Deposited Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A	10.68	51.2	7.28×10^{-10}
B	7.00	51.2	1.69×10^{-9}
C	2.17	51.2	1.76×10^{-8}
D	2.34	51.2	1.52×10^{-8}
E	40.06	8.0	1.28×10^{-10}
F	36.72	8.0	9.62×10^{-12}
G	46.73	8.0	5.94×10^{-12}
H	40.06	8.0	8.08×10^{-12}

Table 5 SEU Sensitivities of Inverter Circuit with Logic 0 Input From Ref. [14].

The third circuit tested was an inverter in the ring oscillator. Its input value was constantly changing between a logic value of 0 and 1. During the verification of the 35 stage ring oscillator, the period of the transitions was measured at 20ns. This equates to a propagation delay of approximately 286 ps per stage, which would allow for a system clock speed of over 2GHz. In an effort to make the detection of an SEU more visible, the oscilloscope was synchronized with the laser pulse. The oscilloscope was then monitored to detect a distortion in the unsynchronized output waveform. It can therefore be assumed that the most sensitive portion of the period was measured at each laser target location. Results of the test are presented in Table 6.

Laser Target Location	**Deposited Charge (pC)**	**Sensitive Area (μm^2)**	**Soft Error Rate (Errors/Day)**
A	0.47	51.2	3.81×10^{-7}
B	0.06	51.2	2.47×10^{-5}
C	0.23	51.2	1.52×10^{-6}
D	0.13	51.2	4.62×10^{-6}
E	0.02	8.0	4.49×10^{-5}
F	0.03	8.0	1.78×10^{-5}
G	0.05	8.0	4.62×10^{-6}
H	0.02	8.0	4.49×10^{-5}

Table 6 SEU Sensitivities of Inverter Circuit Ring Oscillator From Ref. [14].

The fourth circuit tested was a NOR gate in the SEU test circuit with the A and B inputs held at a constant logic 0 value. The oscilloscope was monitored to detect a transition on the outputs. Results of the test are presented in Table 7.

Laser Target Location	Deposited Charge (pC)	Sensitive Area (μm^2)	Soft Error Rate (Errors/Day)
A3	13.35	51.2	4.66×10^{-10}
B3	9.35	61.44	1.14×10^{-9}
C3	6.68	51.2	1.86×10^{-9}
D3	0.13	51.2	4.62×10^{-6}
E3	0.13	51.2	4.62×10^{-6}
F3	0.40	51.2	5.16×10^{-7}
G3	0.27	51.2	1.17×10^{-6}
H3	26.70	8.0	1.82×10^{-11}
I3	33.38	9.6	1.40×10^{-11}
J3	25.04	8.0	2.07×10^{-11}
K3	13.35	16.0	1.46×10^{-10}
L3	16.69	16.0	9.31×10^{-11}
M3	16.69	16.0	9.31×10^{-11}
N3	23.37	16.0	4.75×10^{-11}

Table 7 SEU Sensitivities of NOR Gate with Logic 0 Inputs From Ref. [14].

To determine the soft error rate for a PCML digital system, in a satellite in a geosynchronous orbit, the sensitive surface area (estimated from the circuit layout of the active device) and the deposited charge data are used. The method used is described in detail in Reference [22]. The individual soft error rates can then be summed to obtain an estimate for the entire logic gate.

Tables 4 and 5 clearly demonstrate the pronounced effect the input logic value and whether it is a pull-up or a pull-down transistor have on the gate's sensitivity to an SEU. Similar results have been shown for other types of GaAs logic families [Ref 8]. When the data in Tables 4 and 5 are correlated with Figure 19 (inverter schematic with

test sites annotated) several events can be analyzed. Since a PCML inverter has two complimentary inputs and outputs several variations are present and must be evaluated.

If the charge collection event happens near an off pull-down transistor, the negative charge will collect on the drain. If enough charge collects, the output of the gate will change. Eventually, the charge dissipates, and the voltage (logic value) returns to normal.

If the charge collection event happens near an on pull-down transistor, the positive charge will collect on the drain and dissipate to ground through the transistor. Although the positive charge is being dissipated, the node will become more positively charged and can change states if the SEU is of a high enough magnitude.

If the charge collection event happens near an off pull-up transistor, the positive charge will collect on the negative source. If enough charge collects, the output voltage will change enough to cross the logic threshold.

If the charge collection event happens near an on pull-up transistor, electrons will collect on the positive source and be conducted to V_{DD} via the transistor. However, if the SEU is of a great enough magnitude, the collected charge will be enough to reduce the output voltage of the gate and change the logic threshold.

Based on the data collected during the testing, the pull-up transistors are the most susceptible to a SEU. The pull-up transistor which is off is extremely susceptible to a charge event. Pull-down transistors are not very susceptible to SEUs. The estimated soft error rate for the two inverters tested was 1.92×10^{-5} for a logic 1 on the inputs and 3.54×10^{-8} for a logic 0 on the inputs. [Ref 14]

Table 7, the PCML NOR gate, when correlated with Figure 21 (schematic of the NOR gate with test sites annotated) confirms the results seen during the inverter experiments. The estimated soft error rate for the NOR gate was 1.09×10^{-5}. [Ref 14]

A comparison between Tables 4, 5, and 6 indicates that as the frequency is increased the SEU sensitivity is increased. At all target locations, the SEU susceptibility was lower during the static tests than during the test using the ring oscillator. The effect

of frequency on SEU sensitivity has been noticed with other forms of GaAs logic [Ref 8]. The estimated soft error rate for the ring counter inverter was 1.43 X 10^{-4}. [Ref 14]

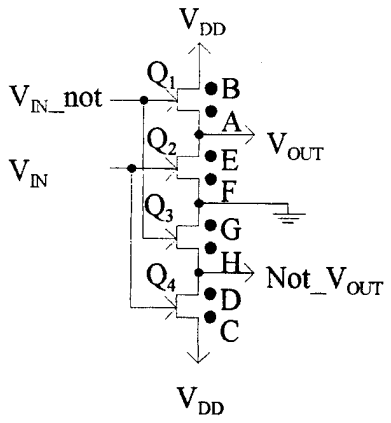


Figure 20 Schematic Diagram of PCML Inverter From Ref. [14].

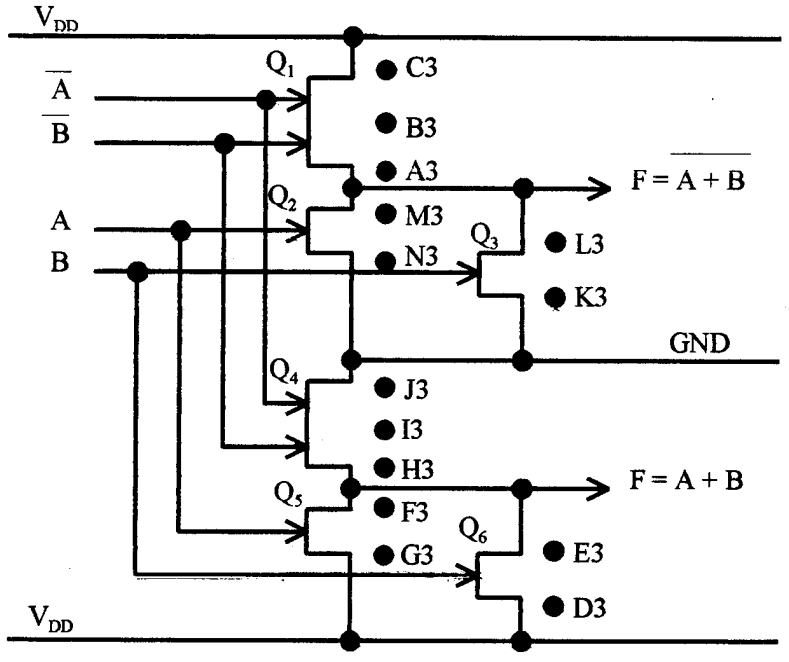


Figure 21 Schematic Diagram of PCML NOR Gate From Ref. [14].

III. PCML GALLIUM ARSENIDE CIRCUIT TESTING

A. BACKGROUND

One of the anticipated effects of PCML's dual-path logic design was that of low static power consumption [Ref 9]. This is due to the fact that V_{DD} is never directly connected to ground. Therefore, there is no static current flow and the logic operates in a manner similar to CMOS. Current only flows when the output state changes. This attribute overcomes the high static current problem associated with DCFL circuits.

PCML was designed to operate with an input rail voltage of 3.3 V. However, PCML's topology is such that it should be able to operate satisfactorily even at lower rail voltages. If operation, at lower rail voltages, was achieved then the power consumption would be further reduced. LT. Wolf and Professor D. J. Fouts felt this could be accomplished without a significant reduction in operating frequency. [Ref 9]

The goal of this testing, therefore, was to fully characterize three PCML circuits; a SEU test circuit (Figure 22), a 35 stage ring oscillator (Figure 23) and a master-slave flip-flop (Figure 24).

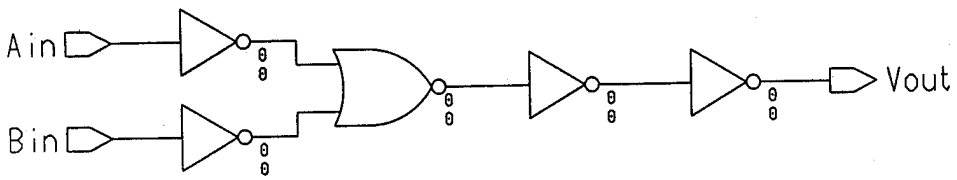


Figure 22 SEU Test Circuit From Ref. [9].

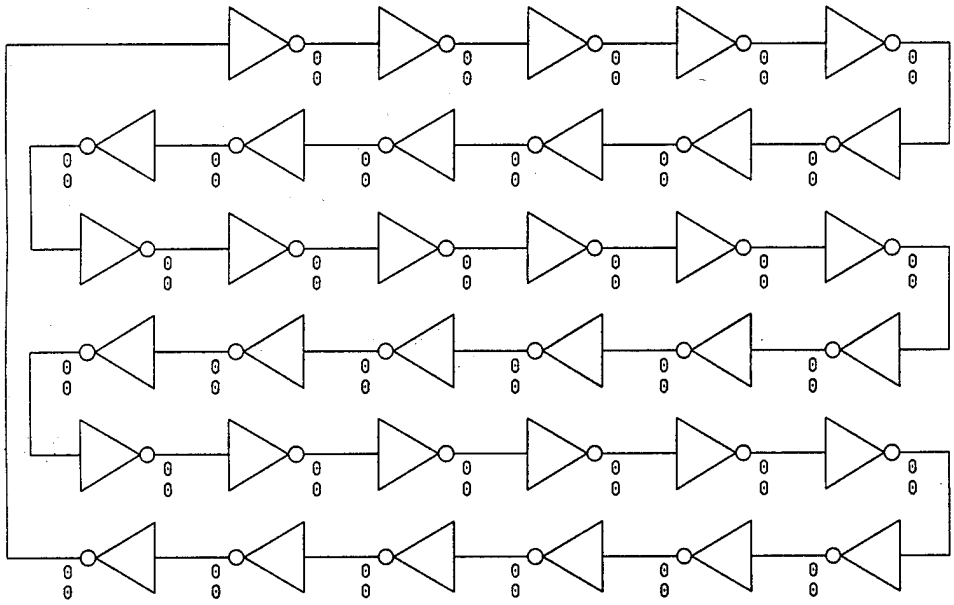


Figure 23 Ring Oscillator From Ref. [9].

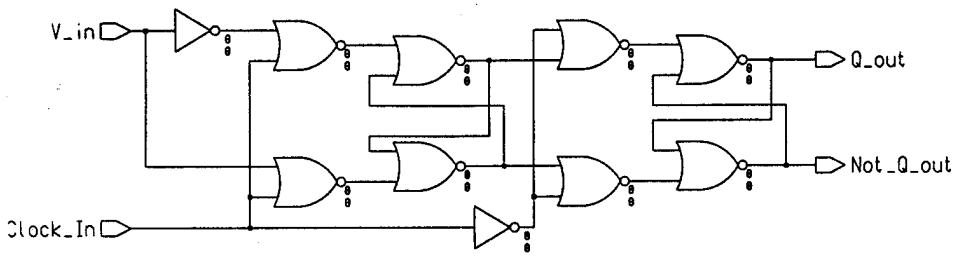


Figure 24 Master-Slave Flip-Flop From Ref. [9].

B. TESTING FIXTURE MODIFICATION

In order to conduct the circuit characterization tests, it was desired to use the same type of test fixture used for the SEU testing. Slight modifications to the wiring would be necessary to allow for source current (I_s) measurements. A duplicate of the SEU test fixture was wired, as previously discussed in the Chapter II, with one basic change. Instead of connecting the V_{DD} and ground connections of the circuits under test to the bottom power and ground rings, a wire was soldered to the top of the test fixture. The wires could then be connected to the appropriate power supplies. A current meter would be placed in series with the power supplies and the currents measured. Figure 25 is a picture of the top of the completed test fixture. The chip was held in place using the same hold down clamp discussed in Chapter II.

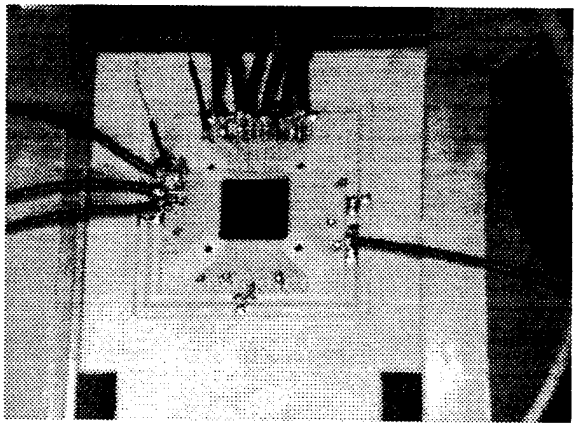


Figure 25 Top of Test Fixture.

C. TESTING PROCEDURES AND EQUIPMENT

The ring oscillator's only inputs were its supply voltages. Initially, the supply voltages were +1.65 for V_{DD} and - 1.65 V for chip ground. These voltages then were reduced to: +/- 1.50 V; +/- 1.25 V; +/- 1.00 V or until the ring oscillator stopped functioning. The layout of the ring oscillator is shown in Figure 26.

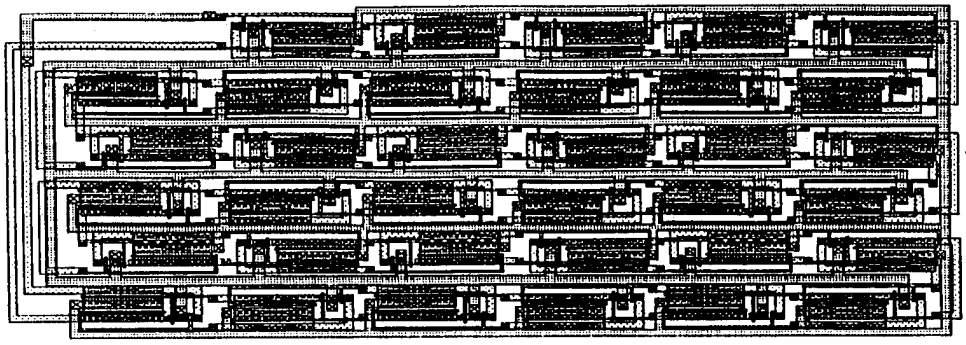


Figure 26 Ring Oscillator Layout From Ref. [9].

The SEU test circuit had its A input connected to a Colby Instruments, Inc. Model PG 1000A 1000 MHZ Pulse Generator and its B input connected to a +1.65 V power supply. The input from the pulse generator was terminated into a 50Ω resistor to minimize reflections. The pulse generator was set to a frequency of 1 GHz with an output amplitude of 1.4 V. A voltage swing from -1.0 V to +0.4 V was used to simulate the correct logic levels. Supply voltages for the chip were +1.65 for V_{DD} and - 1.65 V for chip ground. The layout of the SEU test circuit is shown in Figure 27.

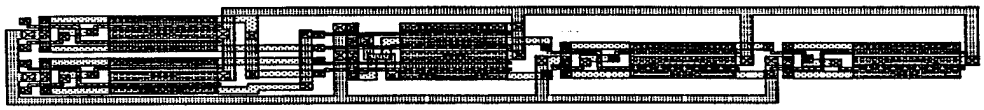


Figure 27 SEU Test Circuit Layout From Ref. [9].

The master-slave flip-flop circuit was designed with the Q NOT output feeding back to the flip-flop's input. This made the flip-flop function as a toggle flip-flop. LT Wolf's [Ref 9] design had two clock inputs vice one clock input and an inverter. The two clock inputs were connected to the pulse generator. The pulse generator has two outputs which are 180^0 out of phase. Each output was set to a frequency of 1 GHz with an output amplitude of 1.4V. A voltage swing from -1.0 V to +0.4 V was used to

simulate the correct logic levels. Supply voltages for the chip were +1.65 for V_{DD} and -1.65 V for chip ground. The layout of the master-slave flip-flop is shown in Figure 28.

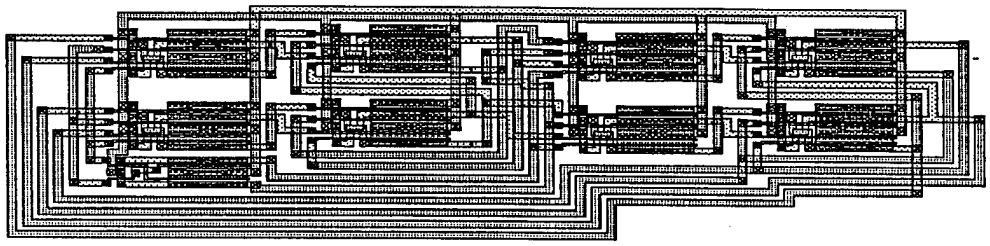


Figure 28 Master-Slave Flip-Flop Layout From Ref. [9].

The output of all the test circuits was measured using a Tektronix 11801A digitizing sampling oscilloscope with a bandwidth of 18 GHz. The outputs were connected to the internal 50Ω terminations to minimize reflections on the output cables. The supply current was measured using a Fluke 8000A/B U Digital Multimeter.

D. TEST RESULTS AND ANALYSIS

The first circuit tested was the ring oscillator. The oscilloscope monitored the A and A NOT outputs with the period, amplitude, maximum and minimum voltages being recorded. The results for the five chips tested are presented in Tables 8A and 8B (Chip E), Table 9 (Chip F), Table 10 (Chip H), and Table 11 (Chip J). Chip D had no ring oscillator output.

Since there are 35 inverters in the ring oscillator, the propagation delay for an inverter can be found by dividing the period by 70 (twice the number of inverters). The average power per gate can be determined by taking the average current times the rail voltage and dividing by 35 (number of inverters). The average propagation delay and power consumption per chip is shown in Table 12.

Supply Voltage	Period (ns)	Amplitude (mV)	Maximum Voltage (mV)	Minimum Voltage (mV)	Source Current (μA)
+/- 1.65 V	7.72	864	304	-856	76.1
	7.43	864	296	-872	76.9
	7.67	872	296	-856	77.2
	7.82	864	304	-872	75.8
	7.68	864	296	-896	76.1
+/- 1.50 V	7.73	920	336	-856	76.0
	7.75	952	336	-856	76.2
	7.74	952	336	-856	75.6
	7.72	952	336	-848	77.0
	7.75	920	336	-848	77.2
+/- 1.25 V	7.77	864	344	-784	49.0
	7.77	872	344	-784	48.3
	7.79	888	336	-784	48.2
	7.79	872	344	-784	48.0
	7.78	880	344	-784	48.1
+/ 1.00 V	8.00	736	280	-672	41.2
	8.24	608	328	-616	41.7
	8.05	792	272	-664	42.4
	8.04	784	272	-672	42.5
	7.95	744	264	-672	42.9

Table 8B Ring Oscillator Outputs for Chip E.

Supply Voltage	Period (ns)	Amplitude (mV)	Maximum Voltage (mV)	Minimum Voltage (mV)	Source Current (μA)
+/- 0.93 V	9.36	624	280	-512	28.5
	9.35	624	280	-512	28.5
	9.39	624	288	-512	28.6
	9.40	624	288	-520	28.6
	9.40	624	288	-520	28.6

Table 8B Ring Oscillator Outputs for Chip E.

(For Chip E, only the A NOT output was available.)

Supply Voltage	Period (ns)	Amplitude (mV)	Maximum Voltage (mV)	Minimum Voltage (mV)	Source Current (μA)
+/- 1.65 V	8.06	776	403	-732	88.7
	8.07	768	404	-724	88.8
	8.08	768	404	-740	89.2
	8.03	784	395	-740	89.7
	8.17	776	404	-732	89.8
+/- 1.50 V	8.10	752	396	-692	75.5
	8.00	768	387	-700	75.2
	8.00	912	387	-708	74.9
	8.04	728	387	-700	74.7
	8.02	904	396	-708	74.7

Table 9 Ring Oscillator Outputs for Chip F.

(For Chip F, only the A output was available.)

Supply Voltage	Period (ns)	Amplitude (mV)	Maximum Voltage (mV)	Minimum Voltage (mV)	Source Current (μA)
+/- 1.65 V	9.92	960	386	-645	42.6
	9.95	952	386	-637	43.0
	9.92	952	387	-638	43.1
	9.90	848	387	-637	42.9
	9.94	856	387	-637	43.5

Table 10 Ring Oscillator Outputs for Chip H.

(For Chip H, only the A NOT output was available.)

Supply Voltage	Period (ns)	Amplitude (mV)	Maximum Voltage (mV)	Minimum Voltage (mV)	Source Current (μA)
+/- 1.65 V	7.84	904	368	-663	35.2
	7.94	888	369	-663	35.3
	7.93	896	369	-663	35.4
	7.95	840	368	-663	35.5
	7.91	896	368	-663	35.4
+/- 1.50 V	7.82	792	360	-663	35.5
	7.84	736	369	-664	35.3
	7.83	784	368	-663	35.2
	7.83	792	368	-663	35.2
	7.84	792	368	-663	35.1

Table 11 Ring Oscillator Output for Chip J.

(For Chip J, only the A NOT output was available.)

Chip Designation	Power Supply Voltages	Average Current (μA)	Average Power (μW/gate)	Average Propagation Delay (ps)
E	+/-1.65 V	2.18	7.21	109
	+/- 1.50 V	2.18	6.55	111
	+/- 1.25 V	1.38	3.45	111
	+/- 1.00 V	1.20	2.41	115
	+/- 0.93 V	0.82	1.52	134
F	+/- 1.65 V	2.55	8.41	115
	+/- 1.50 V	2.14	6.43	115
H *	+/- 1.65 V	1.23	4.01	142
J	+/- 1.65 V	1.01 *	3.33 *	113
	+/- 1.50 V	1.01 *	3.02 *	112
ALL	+/- 1.65 V	2.37	7.81	113
E, F, J	+/- 1.50 V	2.16	6.49	112

Table 12 Average Power and Gate Delay for the Ring Oscillator.

(* indicates values not used in average calculation)

The second circuit tested was the SEU test circuit. The oscilloscope monitored the A and A NOT outputs with the frequency, amplitude, rise time and fall time being recorded. The results for the five chips tested are presented in Table 13 (Chip D), Table 14 (Chip H), and Table 15 (Chip J). Chips E and F had no SEU test circuit output. The average amplitude, rise time, fall time and source current for each chip tested is presented in Table 16.

Output	Frequency (GHz)	Amplitude (mV)	Rise Time (ps)	Fall Time (ps)	Source Current (μA)
A	1.00	152	233	344	178.5
	1.02	152	244	364	178.5
	1.02	152	243	344	178.5
	1.01	152	244	344	178.5
	1.00	152	233	353	178.4
A NOT	1.00	64	347	323	178.6
	1.00	64	407	327	178.6
	1.02	64	292	232	178.6
	1.02	64	367	327	178.6
	1.00	64	307	327	178.7

Table 13 SEU Test Circuit Output for Chip D.

Output	Frequency (GHz)	Amplitude (mV)	Rise Time (ps)	Fall Time (ps)	Source Current (μA)
A	0.992	155	236	398	267
	0.995	154	245	405	266
	1.00	154	235	401	265
	0.995	154	232	402	266
	1.00	153	237	399	266
A NOT	1.00	42	*	*	36.2
	0.992	43	*	*	36.6
	0.997	43	*	*	36.0
	1.00	43	*	*	36.3
	1.00	42	*	*	36.7

Table 14 SEU Test Circuit Output for Chip H. (* indicates no useable data)

Output	Frequency (GHz)	Amplitude (mV)	Rise Time (ps)	Fall Time (ps)	Source Current (μA)
A	1.01	194	235	398	353
	1.01	178	240	403	352
	0.997	190	232	395	353
	0.988	192	237	400	351
	0.992	190	237	399	352

Table 15 SEU Test Circuit Output for Chip J.

Chip Designation	Average Amplitude (mV)	Ave Rise Time	Ave Fall Time	Average Current
D (A)	152	239	350	178
(A NOT) *	64	344	307	178
H (A)	154	237	401	266
(A NOT) *	43	**	**	36
J (A)	188	236	399	352
D, H, J (A)	156	238	383	266

Table 16 Average Power and Gate Delay for the SEU Test Circuit.

(* indicates not used in average calculations, ** indicates no useable data)

The third circuit tested was the master-slave flip-flop circuit. The oscilloscope monitored the A and A NOT outputs with the frequency, amplitude, rise time and fall time being recorded. The results for the five chips tested are presented in Table 17 (Chip F) and Table 18 (Chip J). Chips D, E and H had no flip-flop circuit output. The average amplitude, rise time, fall time and source current for each chip tested is presented in Table 19.

Frequency (MHZ)	Amplitude (mV)	Rise Time (ps)	Fall Time (ps)	Source Current (μA)
499	148	211	406	375
500	148	211	412	374
500	148	219	406	375
500	148	212	406	375
500	148	212	414	375

Table 17 Master-Slave Flip-Flop Output for Chip F.

Frequency (MHZ)	Amplitude (mV)	Rise Time (ps)	Fall Time (ps)	Source Current (μA)
499	110	215	410	577
500	126	218	416	580
495	126	214	418	577
500	126	220	415	578
501	124	219	420	578

Table 18 SEU Test Circuit Output for Chip H.

Chip Designation	Average Amplitude (mV)	Average Rise Time (ps)	Average Fall Time (ps)	Average Current (μA)
F	148	213	409	375
H	122	217	416	578
F, H	135	215	412	477

Table 19 Averages for the Master-Slave Flip-Flop.

Tables 8-12 clearly demonstrates the effect the supply voltage has on the period, amplitude and source current. As the supply voltage is decreased, the period increases and the amplitude and source current decrease. Based on Table 8, PCML circuits should be able to operate with only a power rail of two volts without a significant decrease in performance.

Transient analysis of the PCML inverter indicated an average propagation delay of 108 ps [Ref 9]. The observed average propagation delay in the circuits tested was 113 ps. This is a 18% increase in speed over a DCFL inverter. The average power consumption for a PCML inverter is almost 1/3 of a TDFL inverter. Using the same example used in Chapter I, if an integrated circuit is constructed with PCML gates which dissipate 7.81 μW each and they are placed in a package that can dissipate 10 W, then it

could contain more than 1.2 million transistors. This is a tremendous increase over both DCFL and TDFL circuits.

Tables 13 - 16 demonstrate that PCML circuits are capable of operating at speeds up to 1 GHz (maximum output of the pulse generator). The low output amplitude indicates that the number of complex circuits or gates which could be driven is minimal. This problem can be attributed to the low noise margins and low gain of PCML circuits. These two effects cause PCML circuits to be very susceptible to the body effect. Since this was the first circuit constructed with transistors in series, it is the first circuit to exhibit this problem.

The body effect occurs because the source to substrate voltage is different between transistors. As the substrate voltage increases, the density of the trapped carriers in the depletion layer increases. For charge neutrality to hold, the channel charge must decrease. The resultant effect is that the substrate voltage adds to the channel-substrate junction potential. This increases the gate-channel voltage drop. The overall effect is an increase in the threshold voltage. The increase in threshold voltage leads to a lower output voltage. [Ref 23]

The flip-flop data in Tables 17 - 19 confirm the data collected during the SEU test circuit experiments.

IV. PROPOSED IMPROVEMENTS TO PCML

A. PROBLEM AREAS

Following the SEU testing, it was discovered that the transistor which limited a PCML circuit's effectiveness against the occurrence of a SEU was the off pull-up transistor. The off pull-up transistor's soft error rate accounted for more than 95% of the total soft error rate experienced by the circuit. Therefore, any improvement in SEU susceptibility should be directed toward the effects which cause an SEU in the off pull-up transistor.

The low noise margin associated with PCML circuits, identified by LT Wolf [Ref 9], was one of the problems noted during PCML circuit testing. This coupled with the low gain of the PCML design, caused the amplitude of the output voltage to be reduced in both the SEU test circuit and the master-slave flip-flop. Modification to the basic PCML design to improve gain and noise margins is required. Without an improvement, the ability to drive a large number of gates, in complex circuits is not possible.

B. PROPOSED SOLUTIONS AND INITIAL RESULTS

The SEU susceptibility problem experienced by the off pull-up transistor cannot be corrected with a change to the PCML topology. The effect of a SEU could be minimized in critical operations, by connecting the two complimentary outputs to an exclusive-OR gate. This would allow for the detection of an error. The operation could then be repeated and the corrupted data discarded. If an invalid error was detected, because of a SEU occurring in the exclusive-OR gate, the result would be the operation is repeated. A slight decrease in overall system performance might be experienced, but it should be minimal.

To correct the low gain and noise margin problems, changes to the PCML topology were investigated. Several proposed changes were evaluated using HSPICE to

simulate the circuits. The first change was to place a diode on the gates of the pull-down transistors (Figure 29). This resulted in no improvement in the noise margins or gain. The second proposed change was to place a diode on the gate of all the transistors (Figure 30). Again this resulted in no improvement in the noise margins or gain. The third modification consisted of putting a diode between the drain of the pull-down transistors and ground (Figure 31). This resulted in an overall improvement in the circuit's noise margins and gain when the signal was allowed to propagate through several stages. A spice deck was written to simulate six transistors connected in series and then run using HSPICE. The spice deck file and its results are shown below:

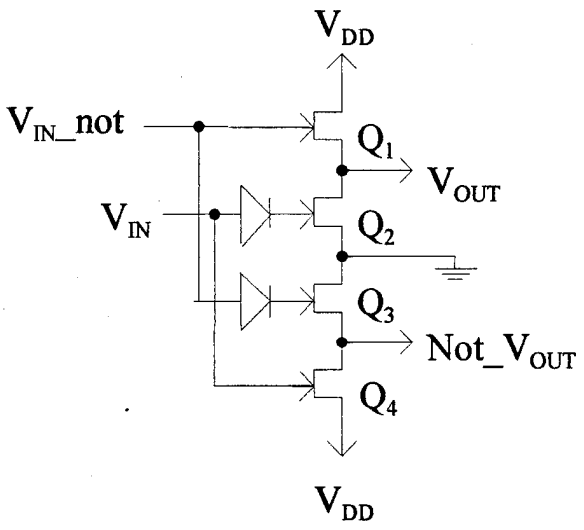


Figure 29 PCML Inverter Modification 1.

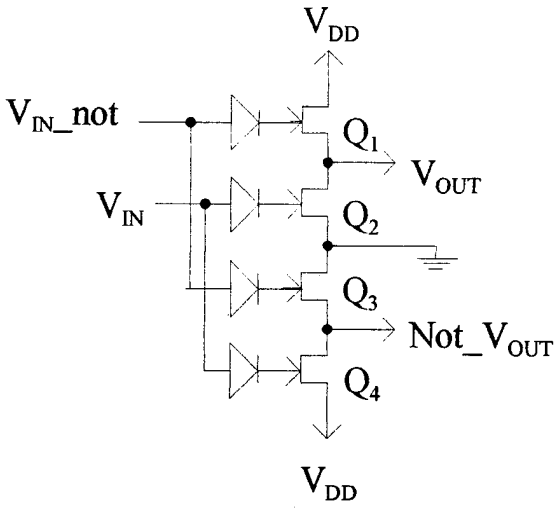


Figure 30 PCML Inverter Modification 2.

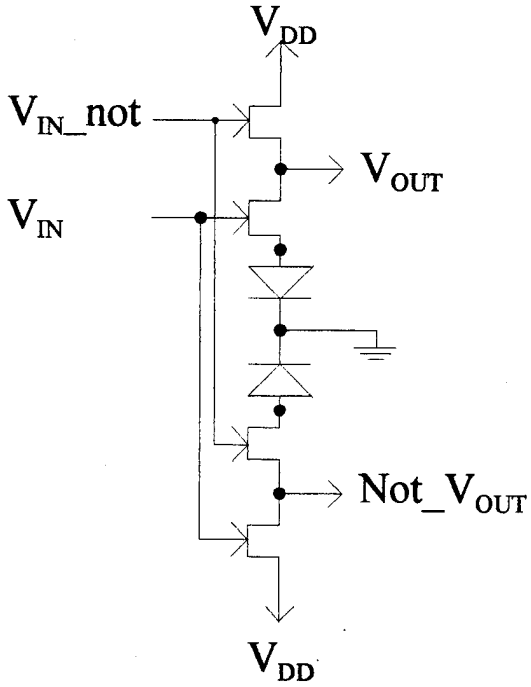


Figure 31 PCML Inverter Modificaton 3.

```
HSPICE file created for circuit pinv2_modified
* Technology: hgaas3mod
*include Vitesse HGaAs3 models and parameters for hspice.
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
*power supply
vds 1 0 3.3
*input signals
vA 101 0
eva_not 102 0 vol='0.7-V(101)'
*main circuit
* NODE: 0 = GND
* NODE: 1 = Vdd
j0 100 101 105 0 enh.1 l=0.8 w=2.4
j1 0 105 0 0 enh.1 l=0.8 w=2.4
j2 0 104 0 0 enh.1 l=0.8 w=2.4
j3 104 102 103 0 enh.1 l=0.8 w=2.4
j4 100 102 1 0 enh.1 l=0.8 w=24.0
j5 1 101 103 0 enh.1 l=0.8 w=24.0
*output loads
j10 110 100 115 0 enh.1 l=0.8 w=2.4
j11 0 115 0 0 enh.1 l=0.8 w=2.4
j12 0 114 0 0 enh.1 l=0.8 w=2.4
j13 114 103 113 0 enh.1 l=0.8 w=2.4
j14 110 103 1 0 enh.1 l=0.8 w=24.0
j15 1 100 113 0 enh.1 l=0.8 w=24.0
j20 120 100 125 0 enh.1 l=0.8 w=2.4
```

j21 0 125 0 0 enh.1 l=0.8 w=2.4

j22 0 124 0 0 enh.1 l=0.8 w=2.4

j23 124 103 123 0 enh.1 l=0.8 w=2.4

j24 120 103 1 0 enh.1 l=0.8 w=24.0

j25 1 100 123 0 enh.1 l=0.8 w=24.0

j30 130 110 135 0 enh.1 l=0.8 w=2.4

j31 0 135 0 0 enh.1 l=0.8 w=2.4

j32 0 134 0 0 enh.1 l=0.8 w=2.4

j33 134 113 133 0 enh.1 l=0.8 w=2.4

j34 130 113 1 0 enh.1 l=0.8 w=24.0

j35 1 110 133 0 enh.1 l=0.8 w=24.0

j40 140 130 145 0 enh.1 l=0.8 w=2.4

j41 0 145 0 0 enh.1 l=0.8 w=2.4

j42 0 144 0 0 enh.1 l=0.8 w=2.4

j43 144 133 143 0 enh.1 l=0.8 w=2.4

j44 140 133 1 0 enh.1 l=0.8 w=24.0

j45 1 130 143 0 enh.1 l=0.8 w=24.0

j50 150 140 155 0 enh.1 l=0.8 w=2.4

j51 0 155 0 0 enh.1 l=0.8 w=2.4

j52 0 154 0 0 enh.1 l=0.8 w=2.4

j53 154 143 153 0 enh.1 l=0.8 w=2.4

j54 150 143 1 0 enh.1 l=0.8 w=24.0

j55 1 140 153 0 enh.1 l=0.8 w=24.0

j60 160 150 165 0 enh.1 l=0.8 w=2.4

j61 0 165 0 0 enh.1 l=0.8 w=2.4

j62 0 164 0 0 enh.1 l=0.8 w=2.4

j63 164 153 163 0 enh.1 l=0.8 w=2.4

j64 160 153 1 0 enh.1 l=0.8 w=24.0

j65 1 150 163 0 enh.1 l=0.8 w=24.0

```
*analysis parameters
.option DCON=1
.option GMINDC=1.000E-09
.option scale=1E-06 post
.dc vA 0.05 0.65 0.01
.end
```

Only one of the complimentary outputs is described in the figures below. The input shown is always connected to A in and the output is always from A NOT. The input voltage (node 101) vs the output voltage (node 100) of the first stage is shown in Figure 32. The input voltage (node 100) vs the output voltage (node 110) of the second stage is shown in Figure 33. The input voltage (node 110) vs the output voltage (node 130) of the third stage is shown in Figure 34. The input voltage (node 130) vs the output voltage (node 140) of the fourth stage is shown in Figure 35. The input voltage (node 140) vs the output voltage (node 150) of the fifth stage is shown in Figure 36. The input voltage (node 150) vs the output voltage (node 160) of the sixth stage is shown in Figure 37.

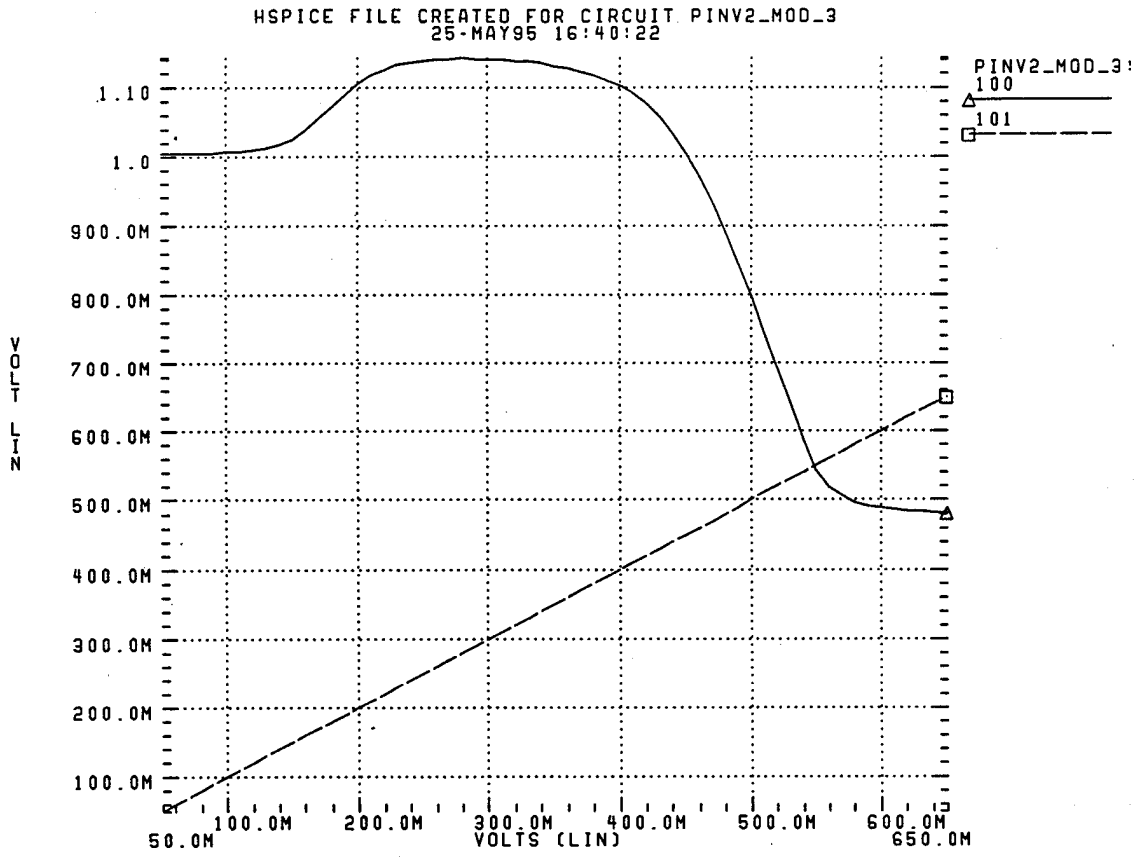


Figure 32 Input Voltage vs Output Voltage of the First Stage.

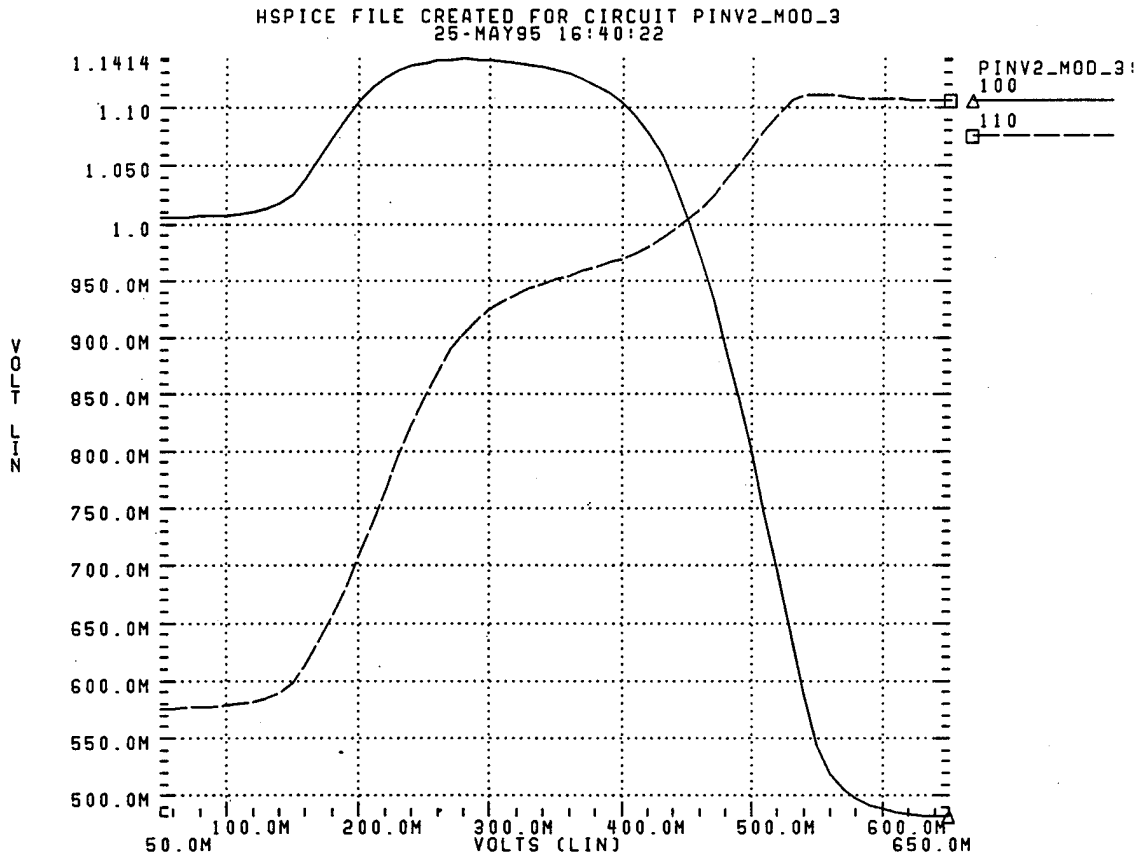


Figure 33 Input Voltage vs Output Voltage of the Second Stage.

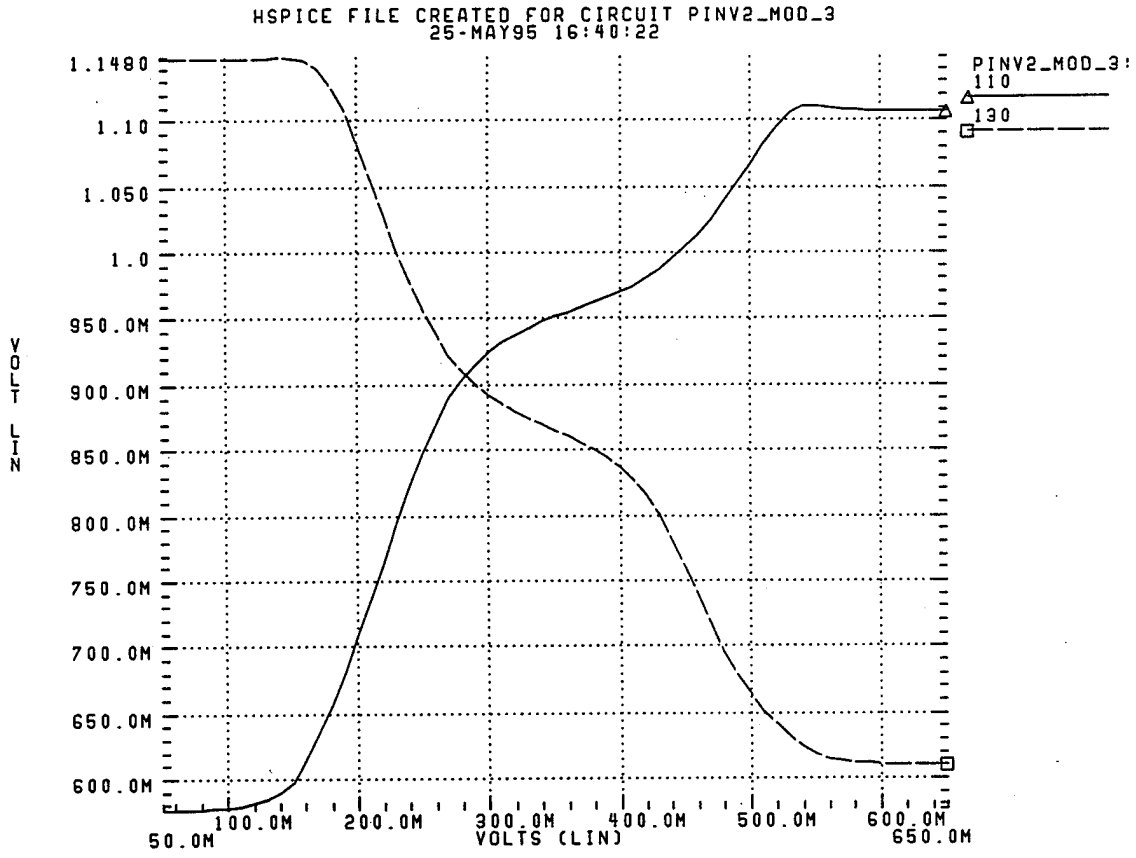


Figure 34 Input Voltage vs Output Voltage of the Thrid Stage.

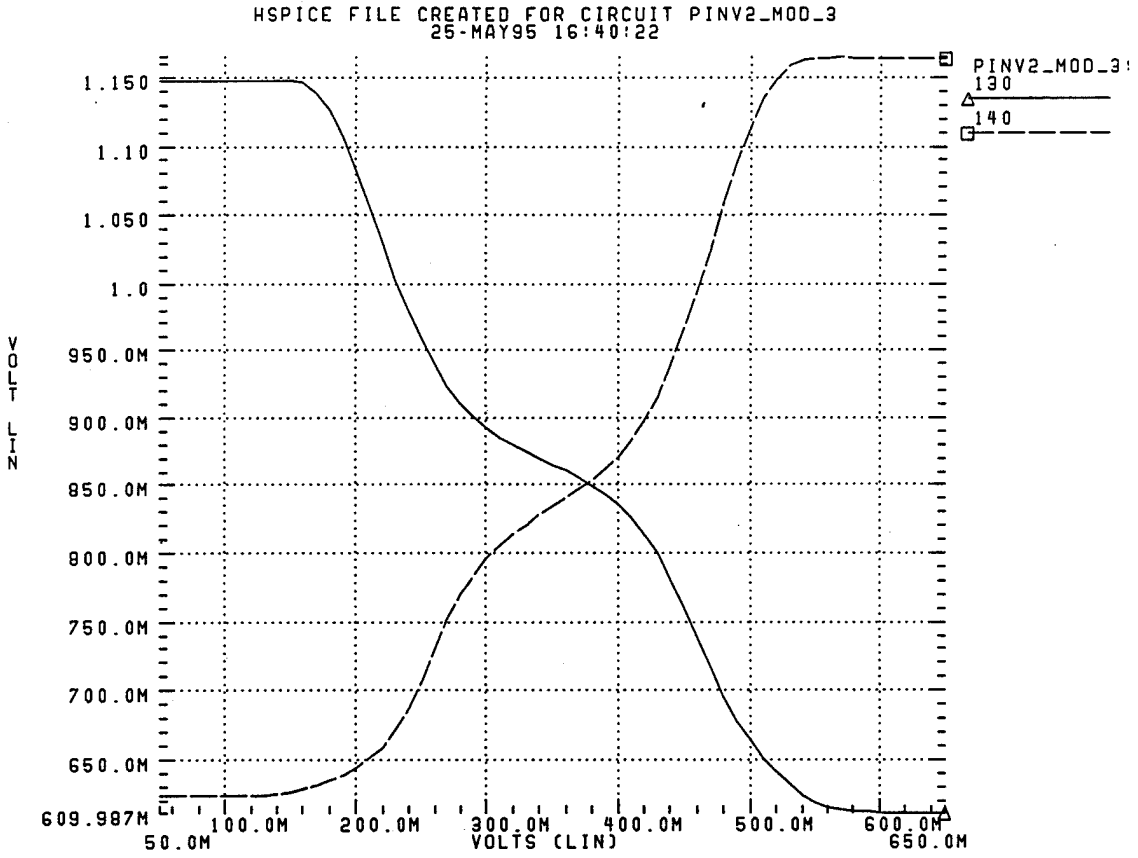


Figure 35 Input Voltage vs Output Voltage of the Fourth Stage.

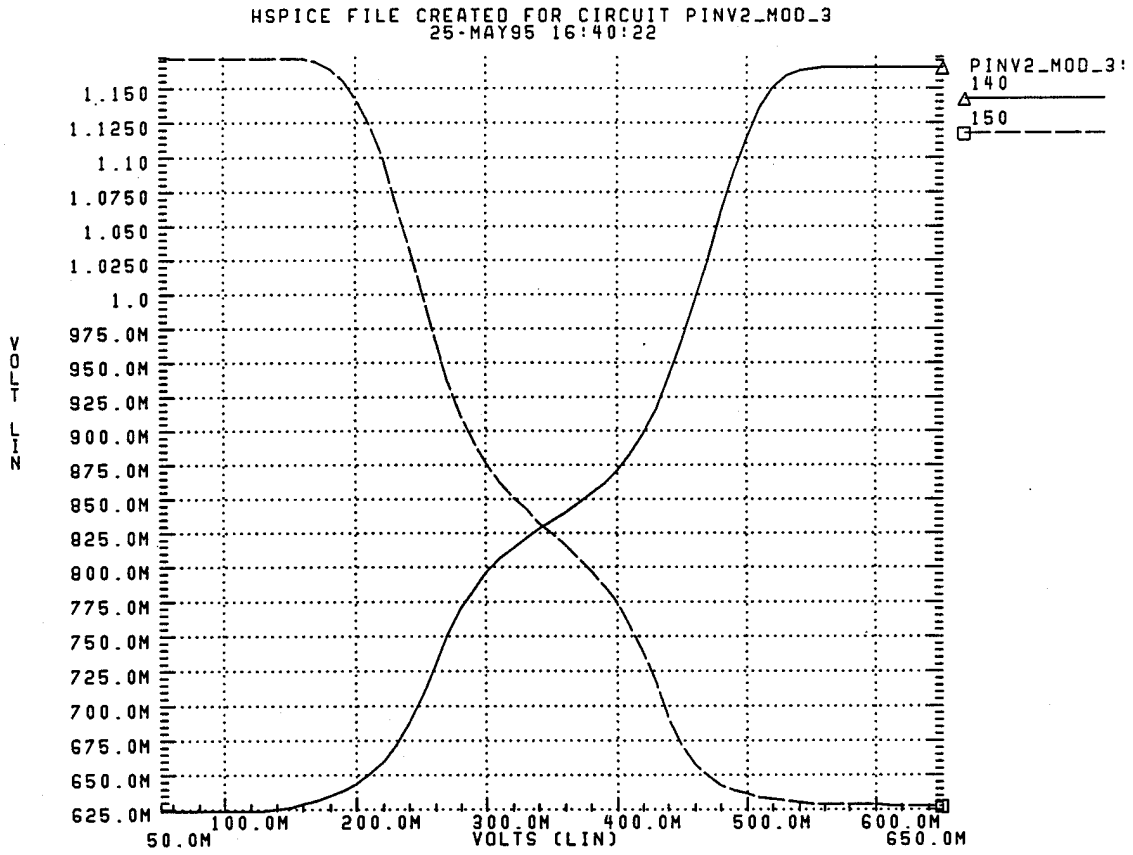


Figure 36 Input Voltage vs Output Voltage of the fifth stage.

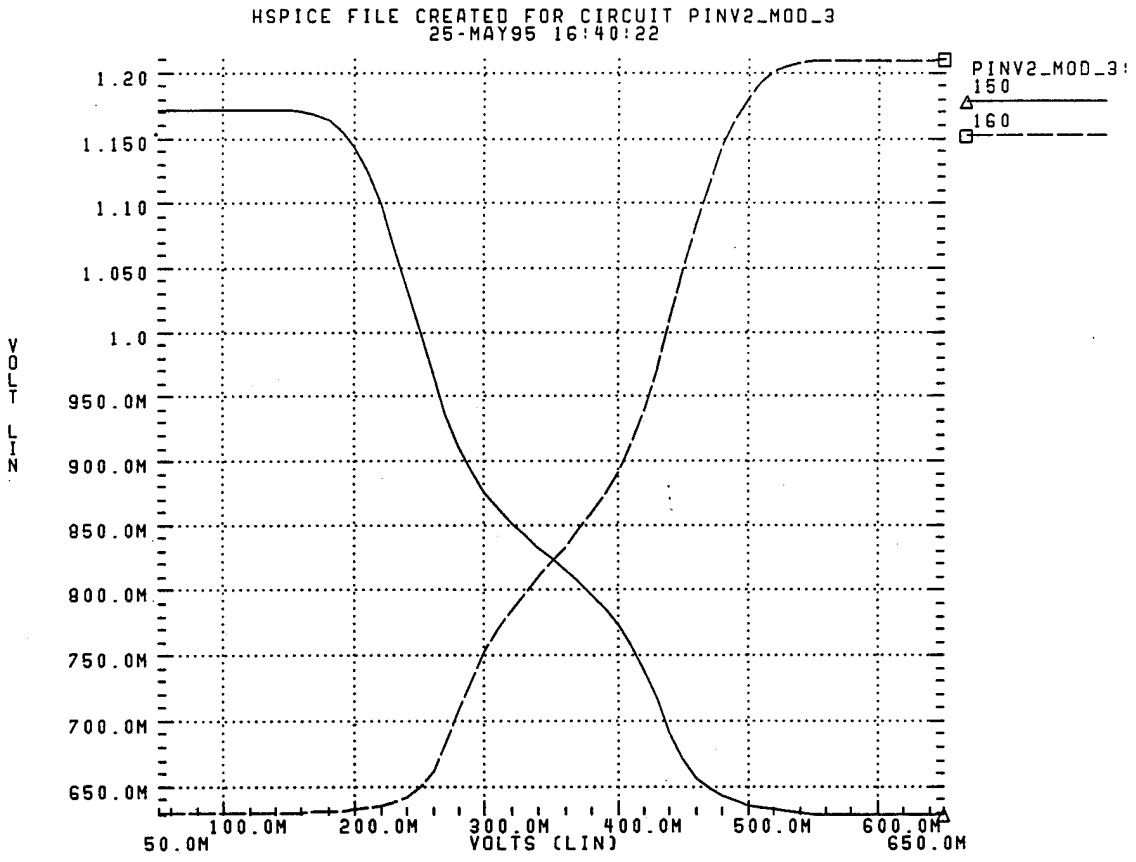


Figure 37 Input Voltage vs Output Voltage of Sixth Stage.

V. COMMENTS AND CONCLUSIONS

A. SINGLE EVENT UPSET TESTING

The first part of this thesis presented the results of single event upset testing on a new gallium arsenide logic family called pseudo-complimentary MESFET logic. The gates tested indicate that this new logic family is less susceptible to single event upsets than direct-coupled FET logic or two-phase dynamic FET logic. This was one of the desires when designing the logic family.

It was found that the off pull-up transistor accounted for more than 95% of a gate's soft error rate. The reasons for this were examined and discussed. A solution, to minimize the effect on critical circuits or outputs, was proposed and the advantages and disadvantages explored.

B. PSEUDO-COMPLIMENTARY MESFET LOGIC CIRCUIT TESTING

The second part of this thesis presented the characterization of three pseudo-complimentary MESFET logic circuits. In respect to propagation delay and power consumption, a pseudo-complimentary MESFET logic inverter provides a shorter propagation delay than a direct-coupled FET logic inverter and a lower power consumption than a two-phase dynamic FET logic inverter. These were two of the goals desired when designing this logic family. Additionally, the pseudo-complimentary MESFET logic inverter demonstrated the ability to operate at a much lower rail voltage than designed. Only a small increase in the propagation delay was experienced, but a further reduction in power consumption was realized.

The testing confirmed a problem with the gain and noise margin of the logic family when used in more complex circuits or gates. A significant reduction in the amplitude of the output voltage was observed. The reduction in the amplitude of the output voltage would prevent the use of a large number of gates or the use of more complex gates. Several changes to the topology where discussed, along with the results of their simulations. Only one topology change (Figure 38) resulted in an overall improvement in the gain and noise margin.

C. RECOMMENDATIONS FOR FUTURE RESEARCH

Further research should be conducted to more fully simulate the proposed topology change to the pseudo-complimentary MESFET logic. If the change does increase the gain and improve the noise margins, a new test and evaluation chip should be fabricated and tested. If further simulations indicate pseudo-complimentary MESFET logic still suffers from inadequate gain and low noise margins, no further research beyond the simulation phase is recommended.

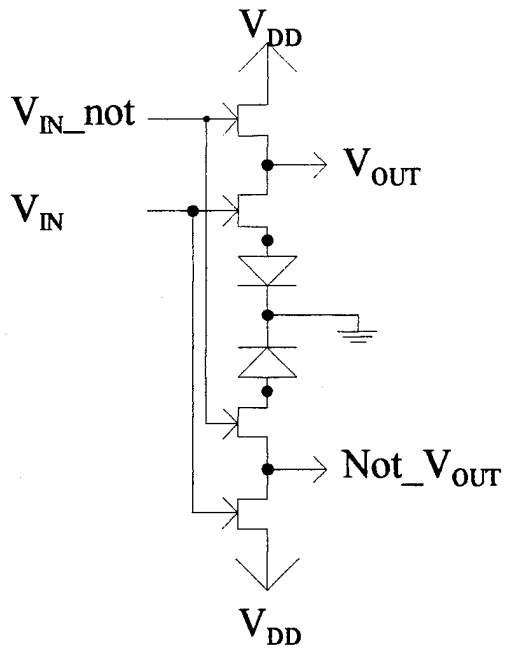


Figure 38 PCML Topology Modification.

LIST OF REFERENCES

1. Sedra, A. S. and Smith, K. C., *Microelectronic Circuits*, 3d ed., p. 384-390 and 970-979, Saunders College Publishing, Fort Worth, TX, 1991.

2. Cray Computer Corporation, *CRAY-3 Hardware Reference Manual*, publication number:3202, CSOS 1.0, copyright 1994.

3. Simons, M., "Radiation Effects in GaAs Integrated Circuits: A Comparison With Silicon," *IEEE GaAs IC Symposium Proceedings*, Phoenix, AZ 1983.

4. Buchner, S. and others, "Charge Collection in GaAs MESFETs and MODFETs," *IEEE Transactions on Nuclear Science*, Vol. 38, No. 6, p. 1370, December 1991.

5. Campbell, A. and others, "Ion Induced Charge Collection in GaAs MESFETs," *IEEE Transactions on Nuclear Science*, Vol. 36, No. 6, p. 2292, December 1989.

6. Weatherford, T. R. and others, "Proton and Heavy Ion Upsets in GaAs MESFET Devices," *IEEE Transactions on Nuclear Science*, Vol. 38, No. 6, pp. 1450-1456, December 1991.

7. Nary, K. R. and Long, S. I., "GaAs Two-Phase Dynamic FET Logic: A Low-Power Logic Family for VLSI," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 10, p. 1364, October 1992.

8. Fouts, D. J. and others, "Single Event Upsets in Gallium Arsenide Dynamic Logic," *IEEE Transaction on Nuclear Science*, Vol. 41, No. 6, pp. 2244-2251, December 1994.

9. Wolf, K., *Radiation Tolerant High Speed, Low Power, Gallium Arsenide Logic*, Masters Thesis, Naval Postgraduate School, Monterey, CA, December 1993.

10. Meta-Software, Inc., *HSPICE User's Manual*, Version H92, Vol. 1-3, Meta-Software, Inc., 1992.

11. University of California at Berkeley, *MAGIC VLSI Circuit Design Software*, Computer Science Division, University of California at Berkeley, CA, December, 1985.

12. Vitesse Semiconductor Corporation, *Parts Manual 1991*, Vitesse Semiconductor Corporation, 1991.

13. Accel Technologies, Inc., *Tango PCB Plus Version 2.1*, Accel Technologies, Inc., 1989-1992.

14. Fouts, D. J. and others, "Single Event Upsets in Gallium Arsenide Pseudo-Complimentary MESFET Logic," paper to be presented at the 32nd Annual International Nuclear and Space Radiation Effects Conference, Madison WI, July 1995.

15. Buchner, S. and others, "Charge Collection from Focussed Picosecond Laser Pulses," *IEEE Transactions on Nuclear Science*, Vol. 35, No. 6, pp 1517-1522, December 1988.

16. Buchner, S. and others, "Laser Simulation of Single Event Upsets," *IEEE Transactions on Nuclear Science*, Vol. 34, No. 6, pp 1228-1233, December 1987.

17. Schneiderwind, R. and others, "Laser Confirmation of SEU Experiments in GaAs MESFET Combinational Logic," *IEEE Transactions on Nuclear Science*, Vol. 39, No. 6, pp 1665-1670, December 1992.

18. Buchner, S. and others, "Charge Collection in GaAs MESFETs and MODFETs," *IEEE Transactions on Nuclear Science*, Vol. 38, No. 6, pp 1370-1376, December 1991.

19. McMorrow, D. and others, "Picosecond Charge-Collection Dynamics in GaAs MESFETs," *IEEE Transactions on Nuclear Science*, Vol. 39, No. 6, pp 1657-1664, December 1992.

20. McMorrow, D. and others, "Fast Charge Collection in GaAs MESFETs," *IEEE Transactions on Nuclear Science*, Vol. 37, No. 6, pp 1902-1908, December 1990.

21. Melinger, J. S. and others, "Critical Evaluation of the Pulsed Laser Method for Single Event Effects Testing and Fundamental Studies," *IEEE Transactions on Nuclear Science*, Vol. 41, No. 6, pp 2574-2584, December 1994.

22. Petersen, E. L. and others, "Suggested Single Event Upset Figure of Merit," *IEEE Transactions on Nuclear Science*, Vol. NS-30, No. 6, pp 4533-4539, December 1983.

23. Weste, N. and Eshraghian, K., *Principles of CMOS VLSI Design: A Systems Perspective*, pp. 51-55, Addison-Wesley Publishing Company, Reading, MA, 1994.

INITIAL DISTRIBUTION LIST

		No. Copies
1.	Defense Technical Information Center Cameron Station Alexandria, Virginia 22304-6145	2
2.	Library, Code 52 Naval Postgraduate School Monterey, California 93943-5101	2
3.	Chairman, Code EC Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
4.	Douglas J. Fouts, Code EC/FS Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	2
5.	Herschel H. Loomis, Code EC/LM Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
6.	LCDR. Steven E. Van Dyk 8932 South Claremont Avenue Chicago, Illinois 60620	2